- PSoC & Switched Cap

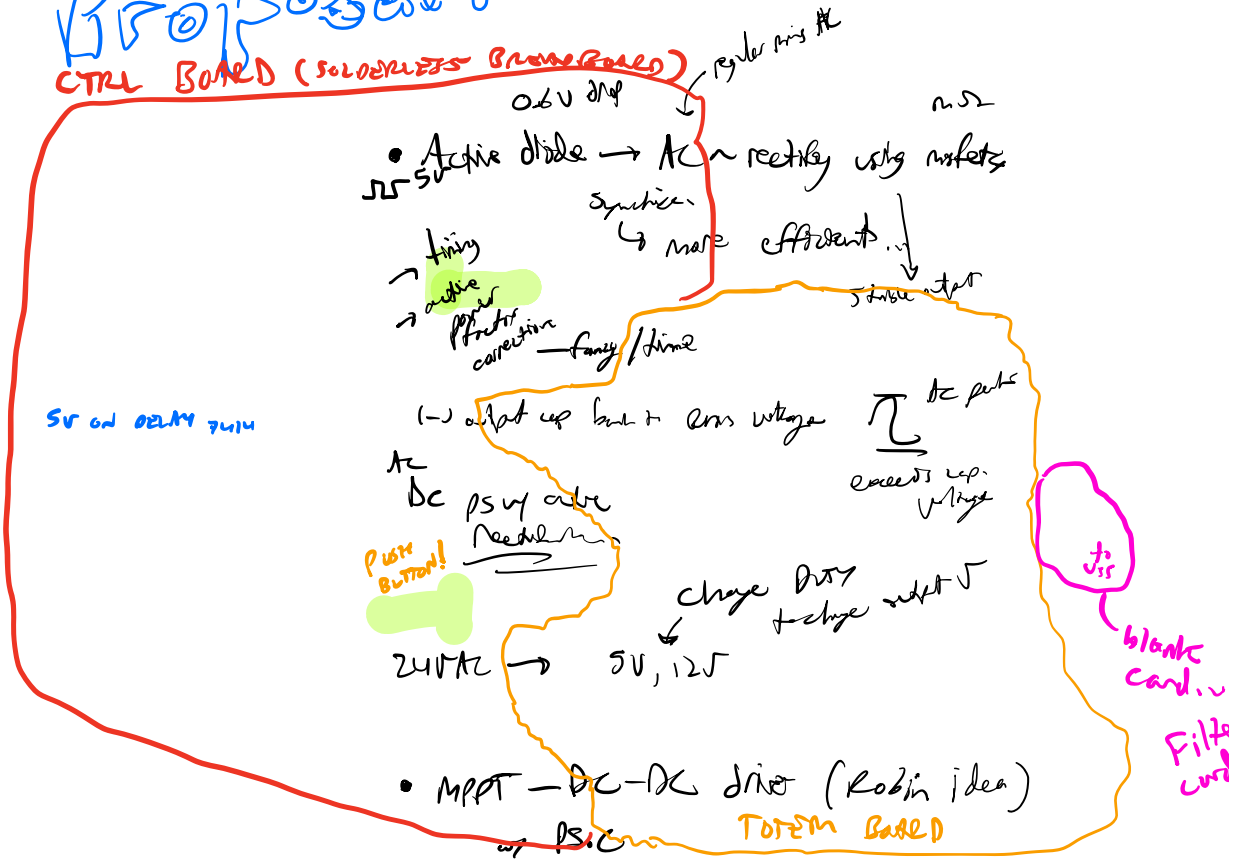
if PSoC etc. piece doesn't work - the other pieces should <u>modular</u>

& idea w/ teeth.

MPPT

mpja
digikey
arrow
allelectronics
sparkfun
adafruit

Project Proposal!



Design Heuristic 1: post pump → largest stack ?

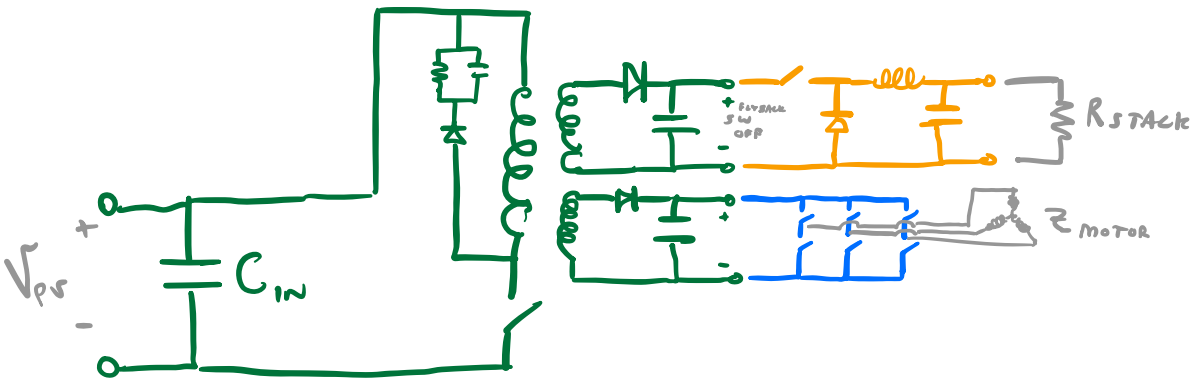
2: sufficient pump ← largest stack

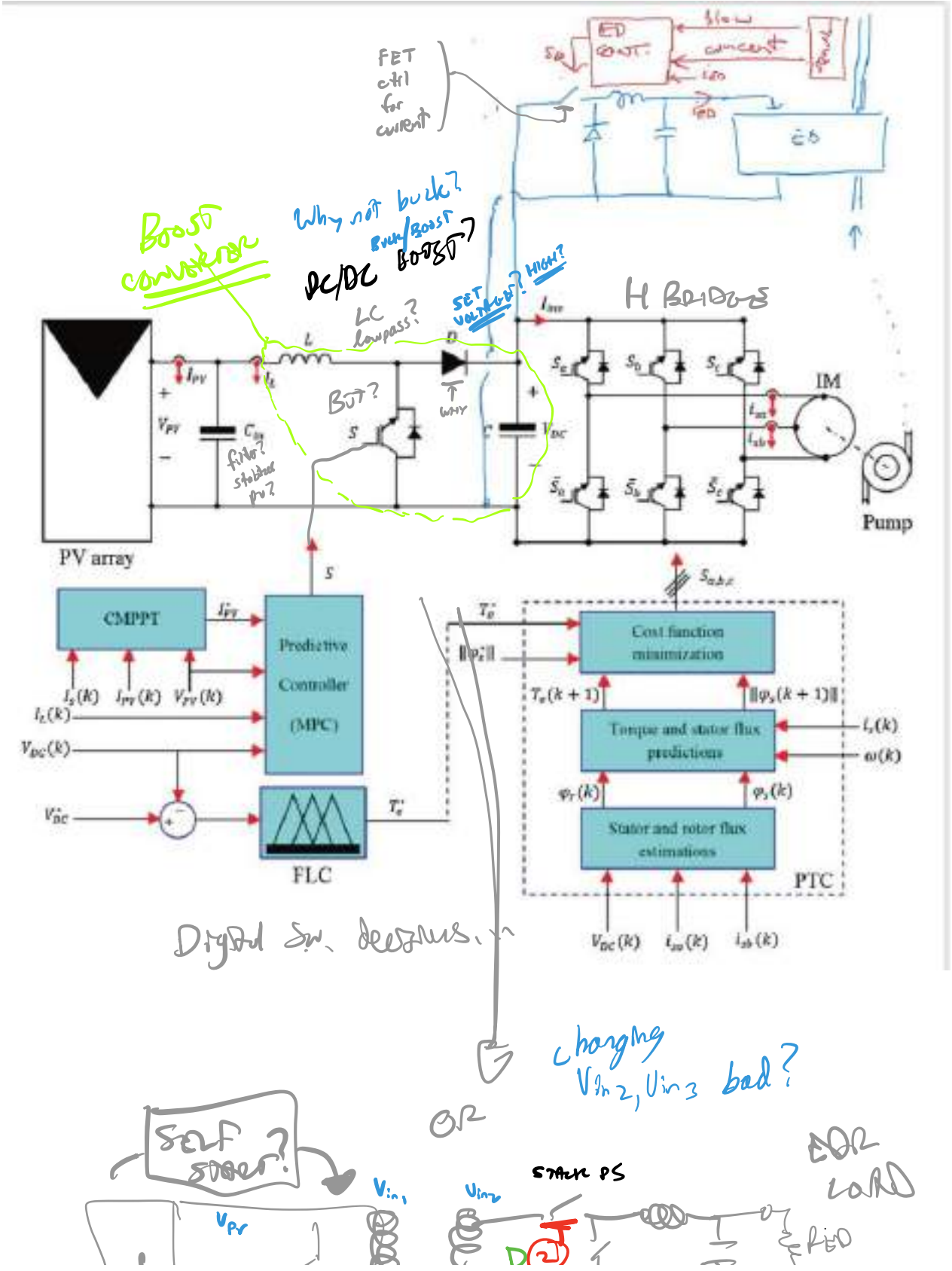
Performance?

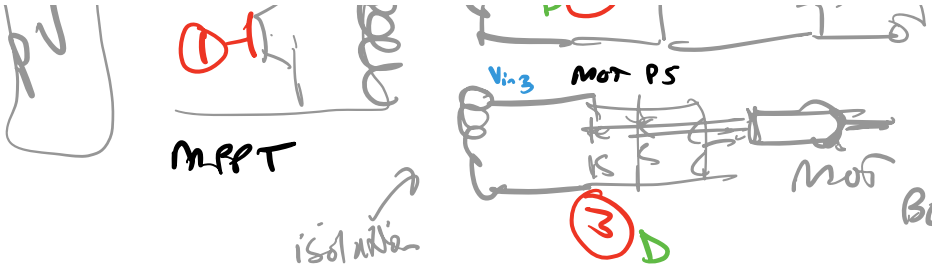
* PRODUCTION * CAPEX BANDWIDTH SEC

1

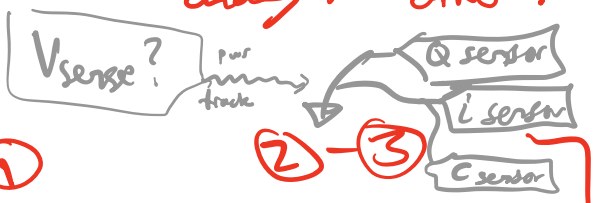
2




FET ctrl for current
Boost converter
Why not buck?
Buck/Boost
DC/DC
LC lowpass?
SET VOLTAGE? HIGH?
H BRIDGE
IM
Pump
PV array
BUT?
WHY
fixed? stabilize pv?
CMPPT
Predictive Controller (MPC)
FLC
Cost function minimization
Torque and stator flux predictions
Stator and roter flux estimations
PTC
Digital sw. designs...
charging
Vin2, Vin3 bad?
OR
SELF START?
Vin1
Vin2
START PS
Vpv
LOAD
RED



ctrl gets 1, 2, 3 from digital signal to analog to drive.



PASO SW for sensor 2, C

1 from power tracks?

MPPT alg.? how does this work? CCM

2, 3 as ctrl for MPPT adjust

from ilim / model based?

PSOC for digital control (speeds? freq.?)

What happens if I SW back? @ 2, 3?

↳ ✓ just pulled down from whatever is there...?

↳ can't ever pull it to Vin...?

"FULLY D.D"

How do we decide 1, 2, 3 speeds?..

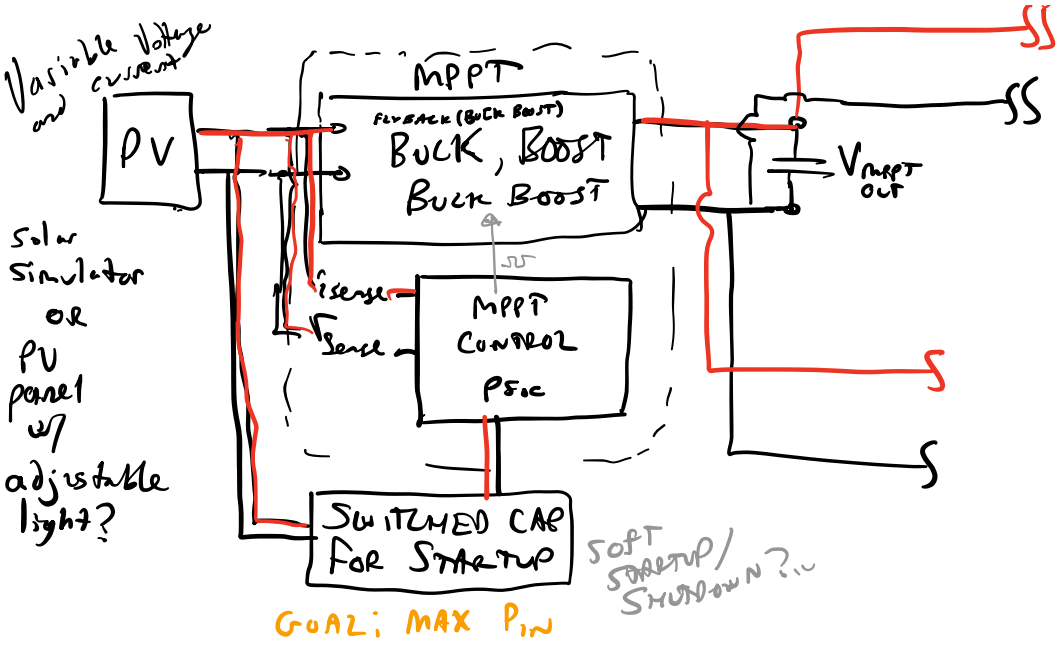
Do @ small scale to prove can work...

↳ scaling ops for large scale

RQ POWER

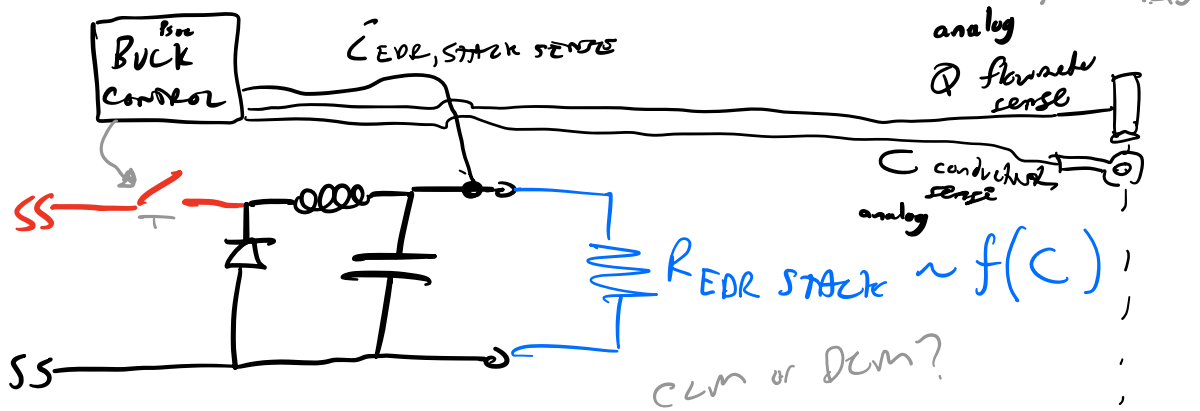
(+) coupled ctrl

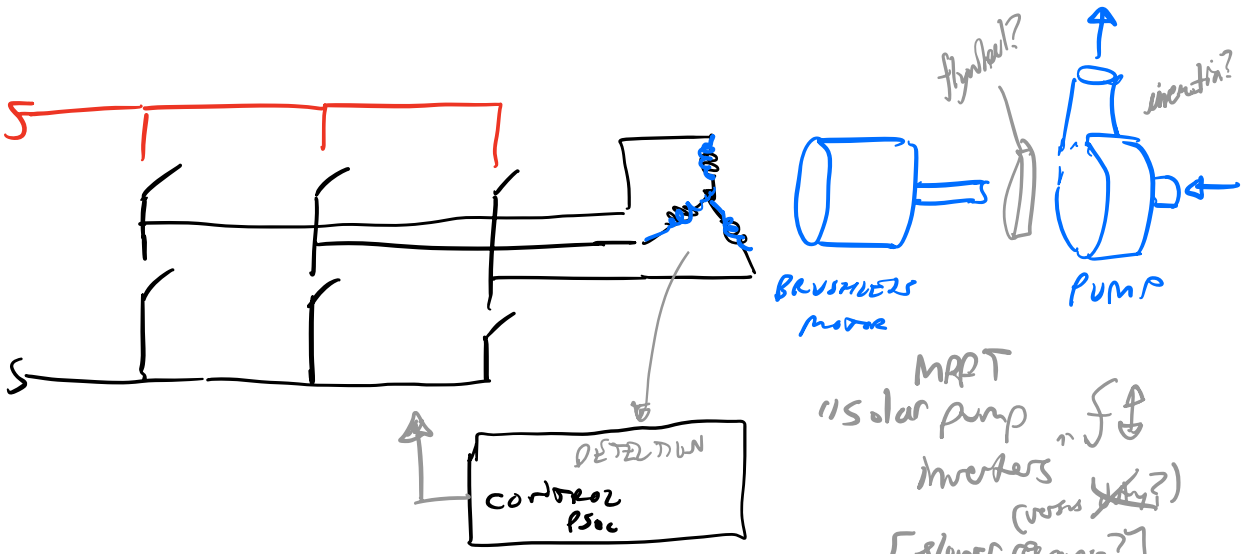
AIM IS TO PROVE CTRL → NOT TO OPT, RQ



GOAL: MAX P_{IN}

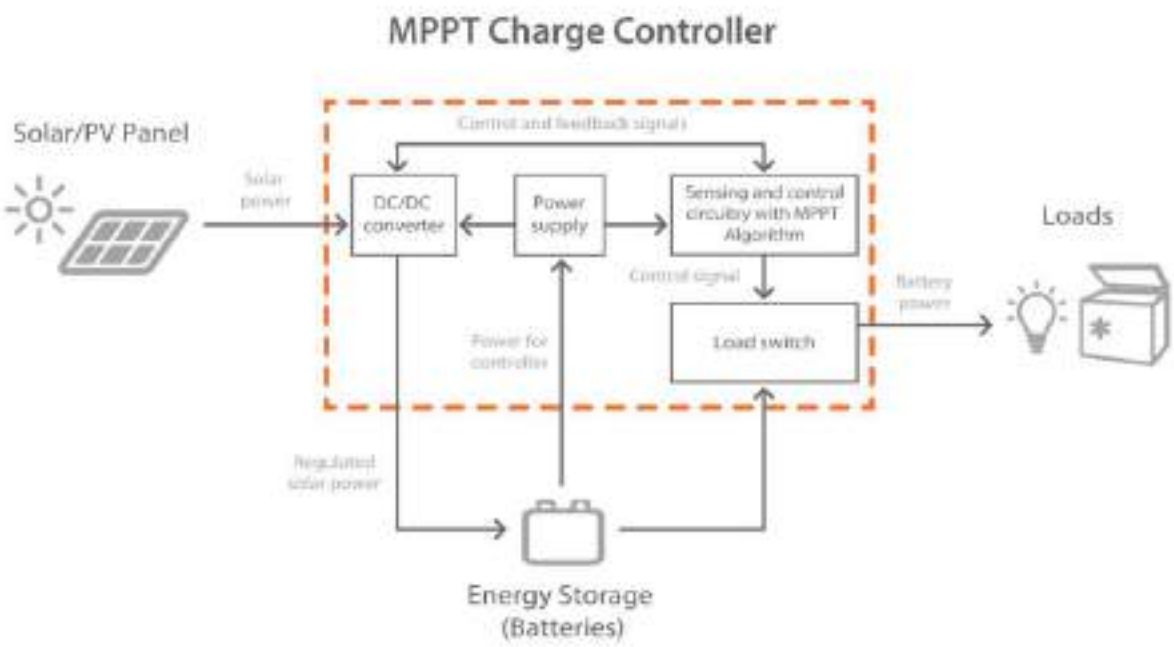
GOAL: MAINTAIN $i_{lim} = f(C, Q)$ — cmd duty 10-90% (regardless of V_{in}, stack PS)

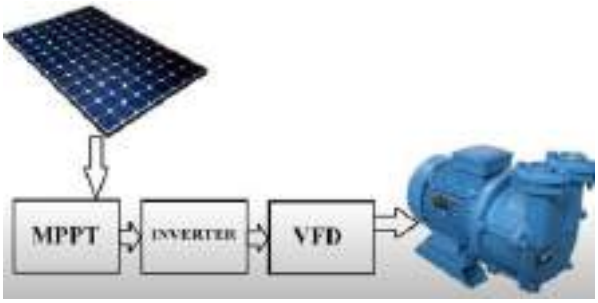




MPPT "solar pump inverters" ~ f_{sw} (varies duty?) [slower response?]

GOAL: MEET P_{IN} / MAINTAIN P_{IN} W/ LEFTOVERS?



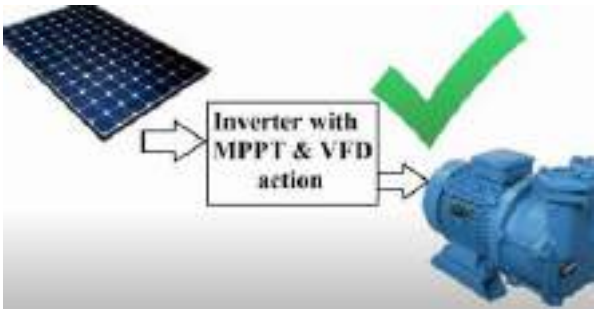


IGBT > MOSFET

for η, high current
high V

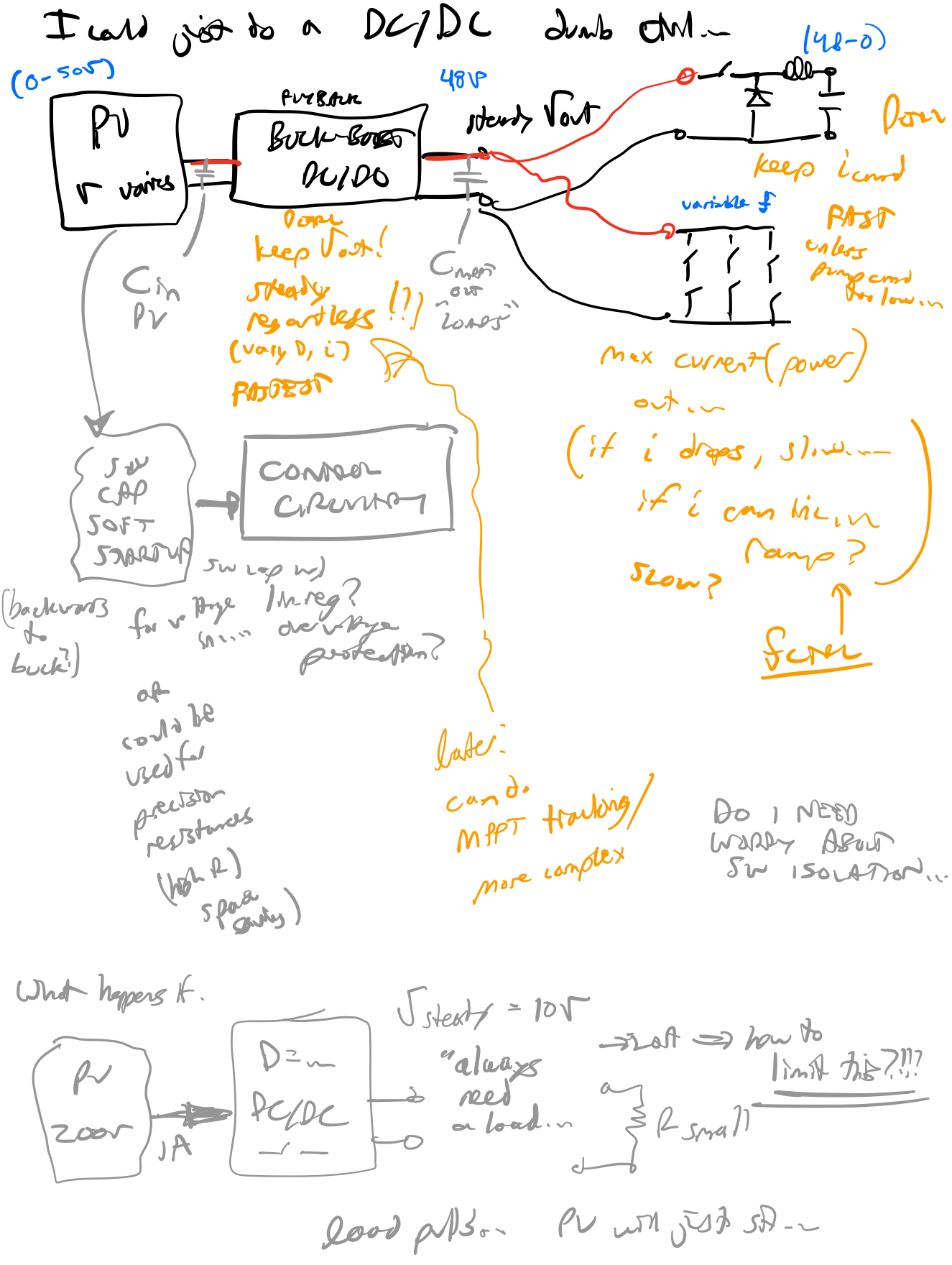
good fast switching

heat dissipation !!!

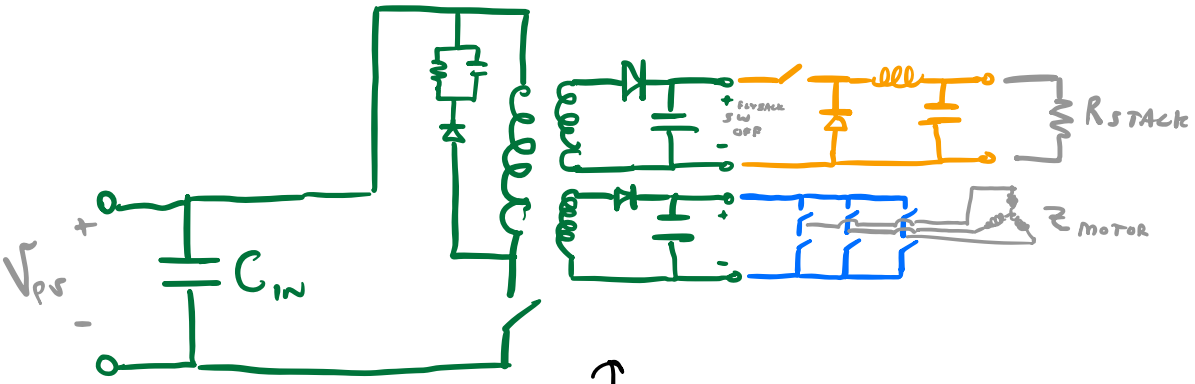


https://www.youtube.com/watch?v=NLrpxi5LqYw&ab_channel=MediElectronics

- input voltage regulation (max power point)
- output V regulation ← feedback circuit...



load pulls... PV will just sag...



related

just one HV coil?

PC coil stack?

only 2 pot wires

T, P

carbon paper w/ electrolyte

simple?

Elec ctrl

Pump ctrl test?

switched?

ZMDC → valve, ctrl, encoder, therm

passive

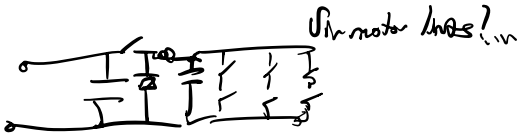
self-regulating flow?

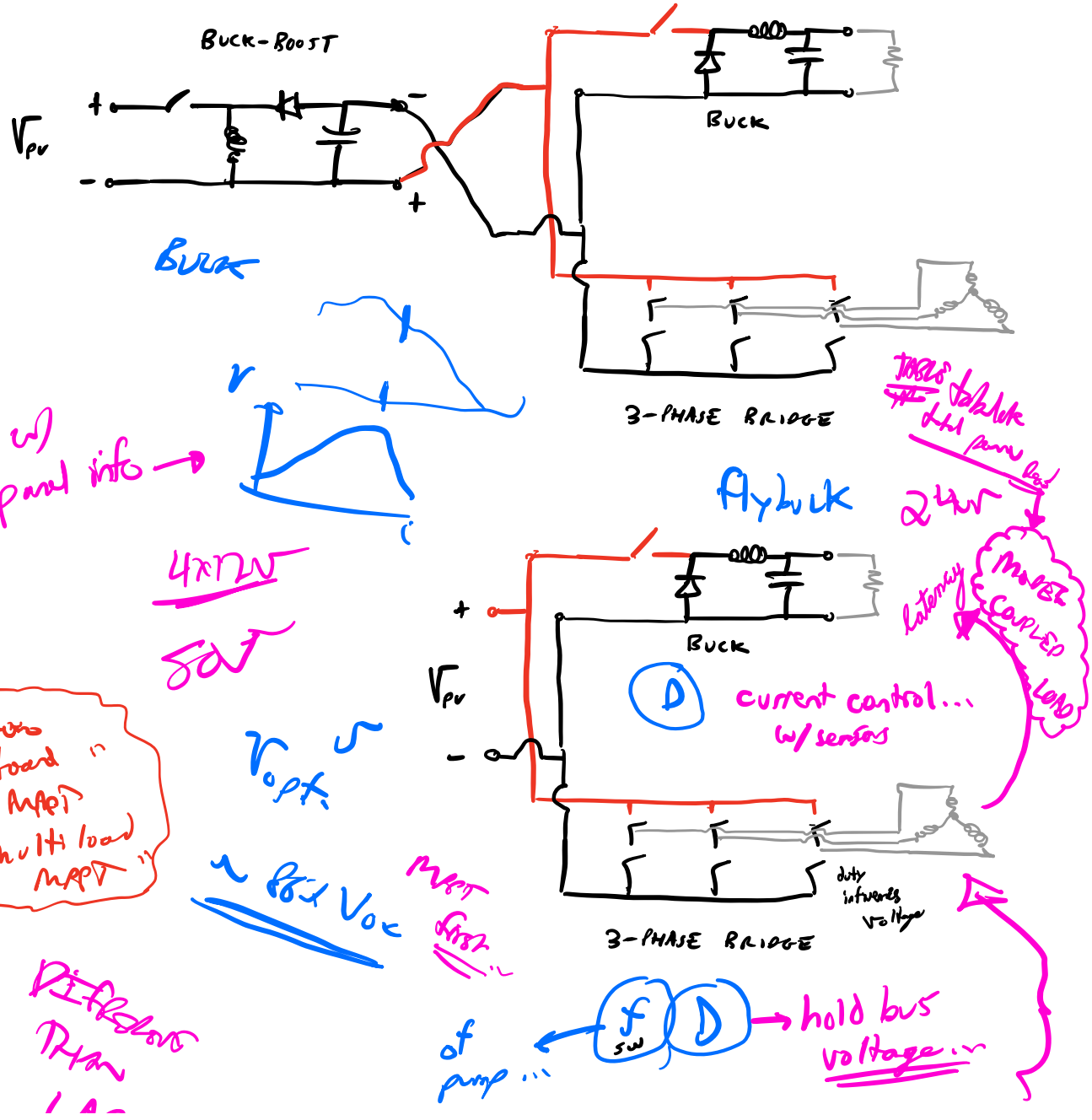
Psense

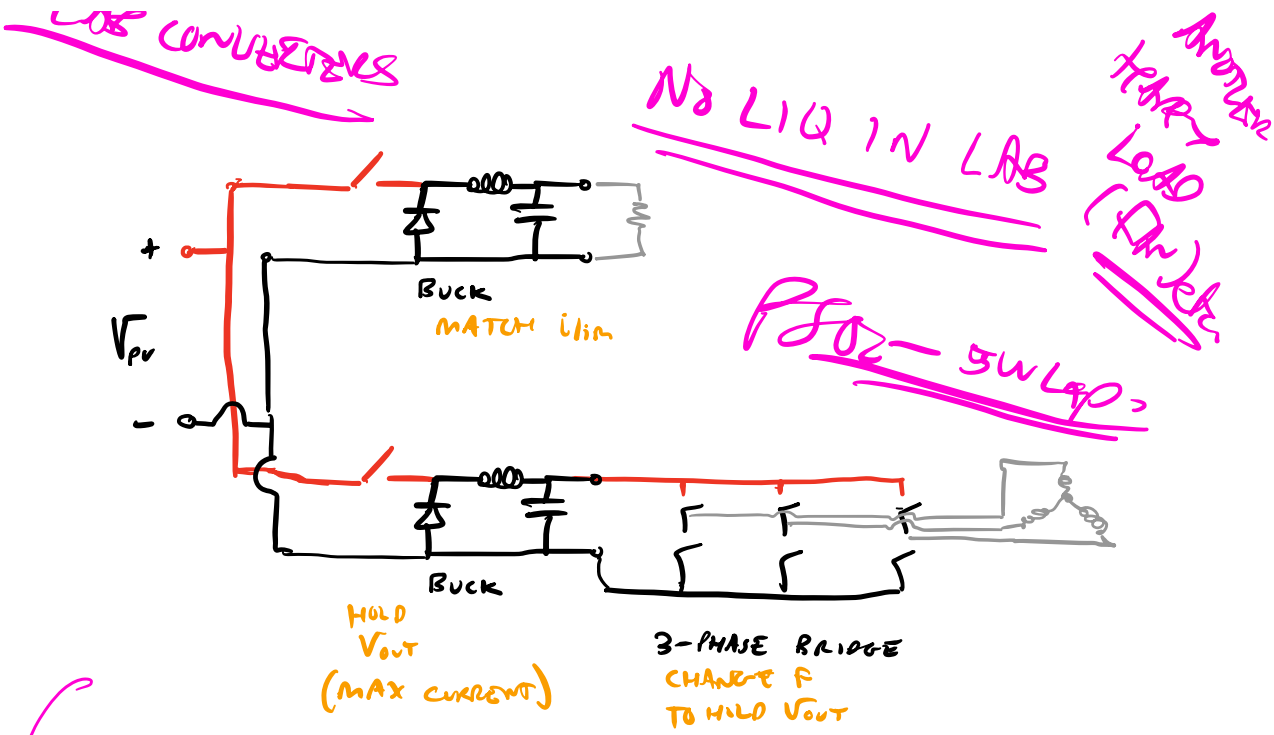
Manifold

Prog.

Prop. valve sets flow based on other stream...







Get ratings / DRS (ΔV etc.)

V_{in}

Model Load!

V_o stack 0-36VDC → 1A?
V_o pmp 24VDC? 2A

Digitally programmable variable resistor?

stacks behavior vs.

C, i, Q

AC R

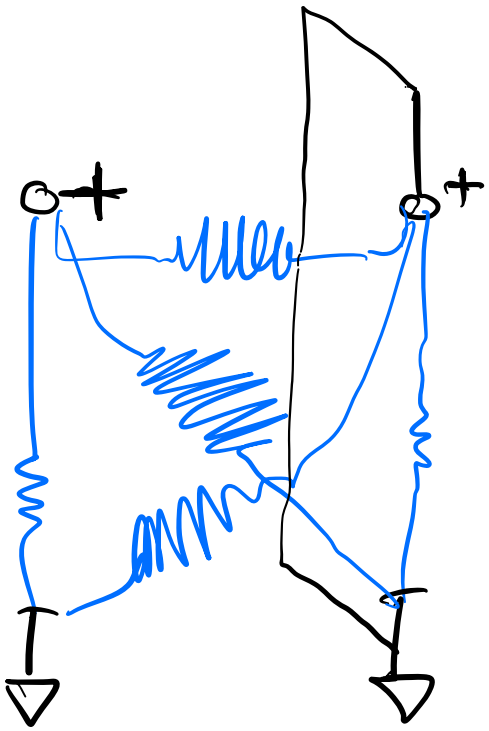
Cost

for homescale

just 2 bucks

PSoC power? –

0-50 PV

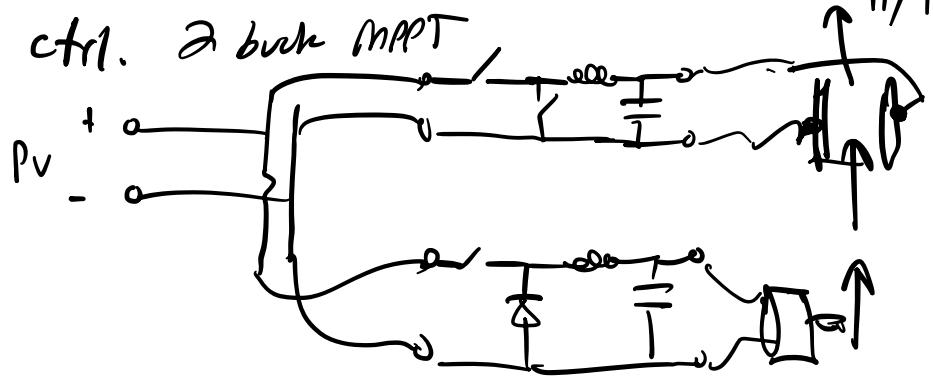


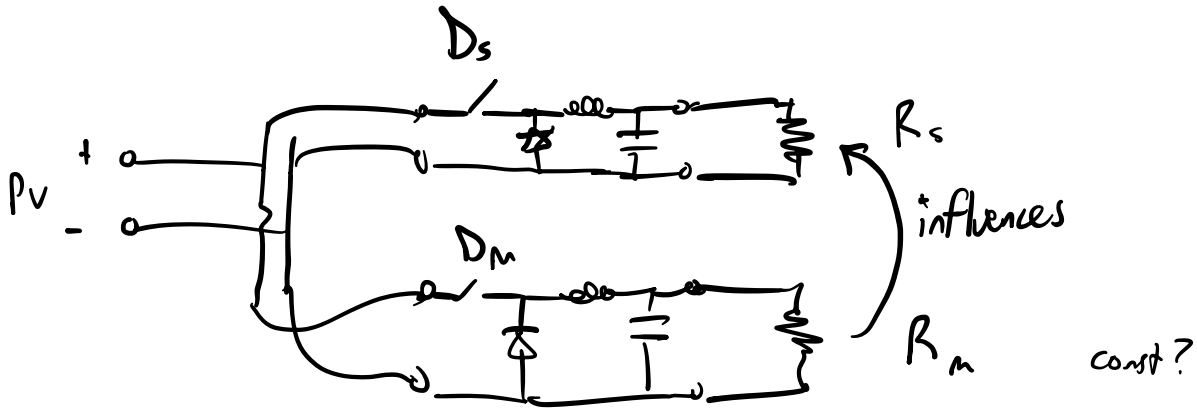
https://www.ti.com/lit/an/snva674c/snva674c.pdf?ts=1698876769581&ref_url=https%253A%252F%252Fwww.bing.com%252F

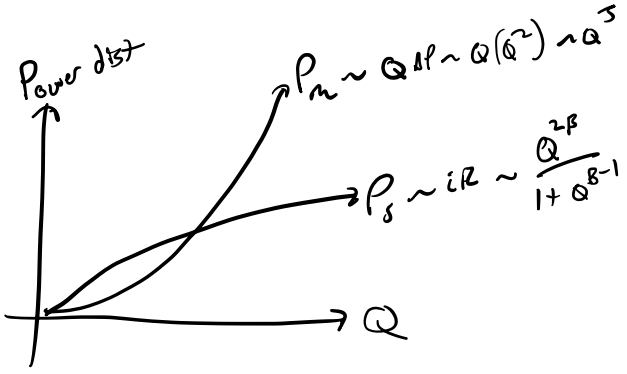
Fly Buck Converter

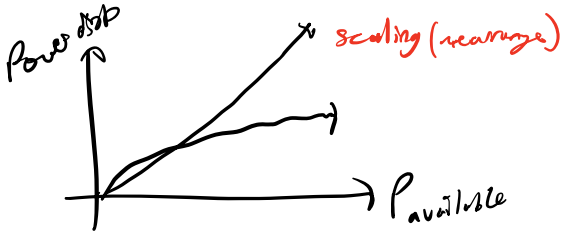
11/14/23

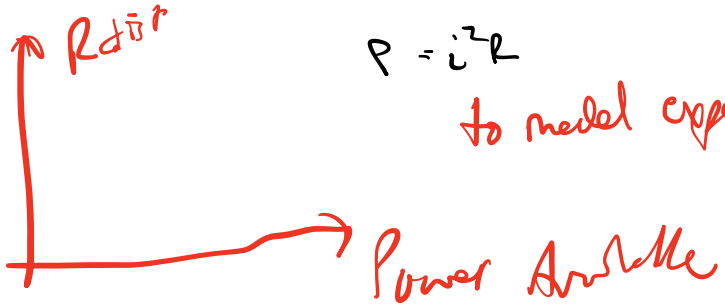
ideal ctrl. 2 buck MPPT







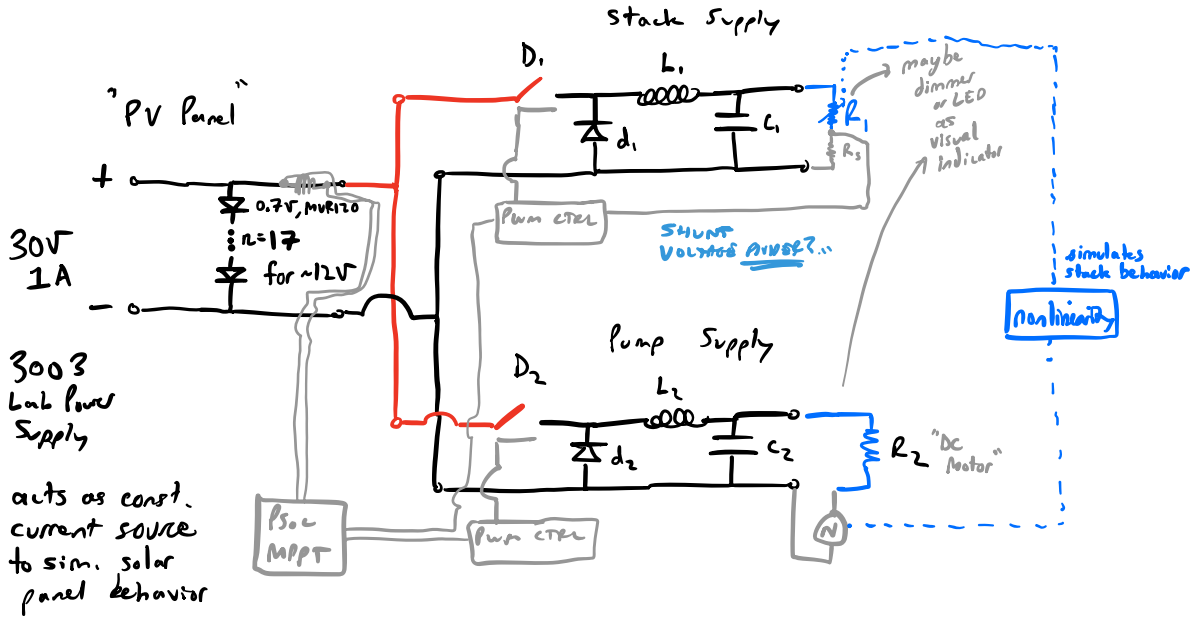


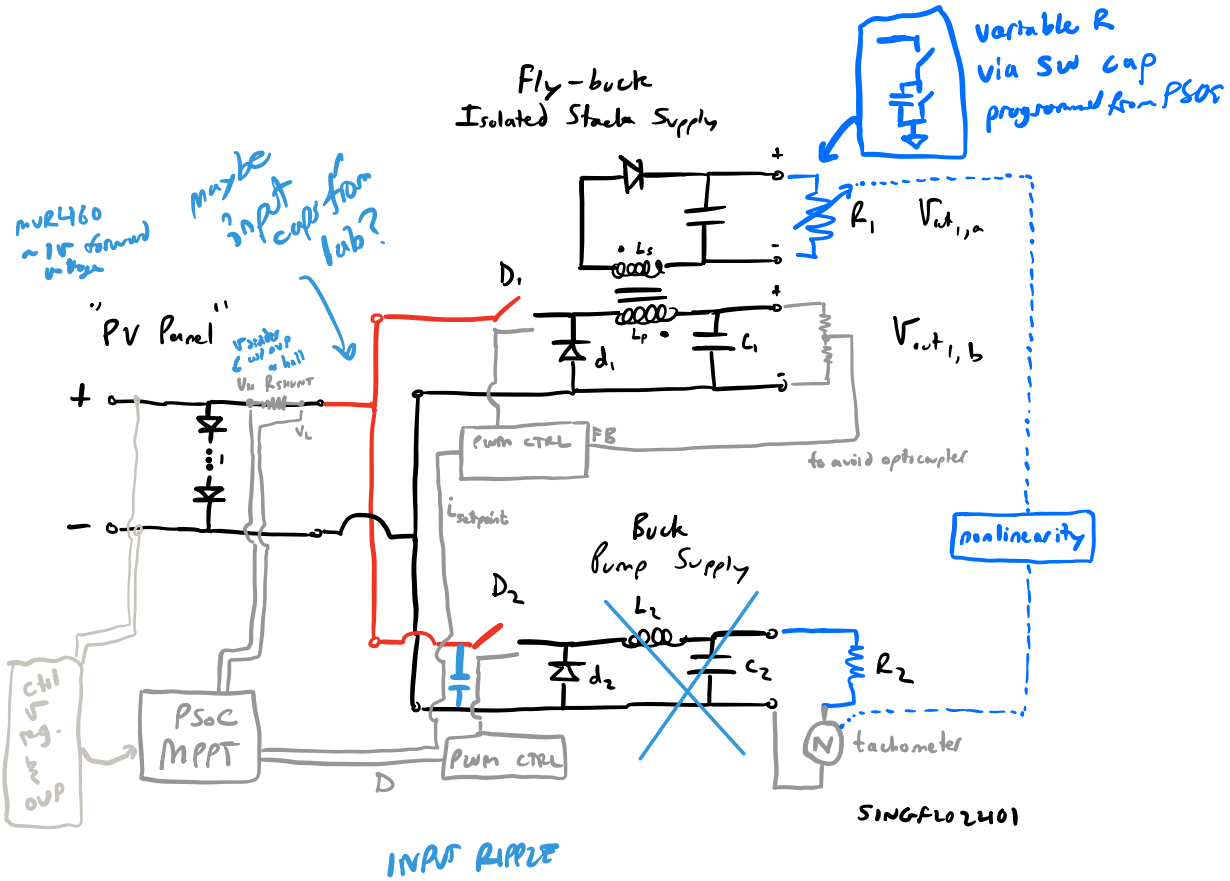


$P = i^2R$

to model expected R variance
(optimal power distribution)

ARCHITECTURE





DESIGN REQUIREMENTS

small scale EDR

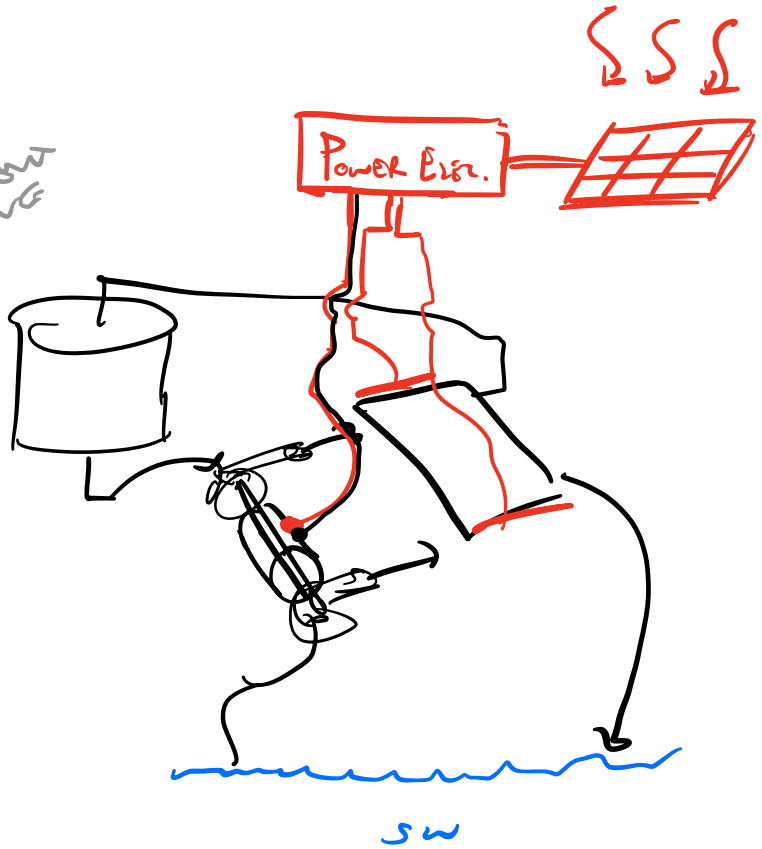
D 0.4 D 0.8

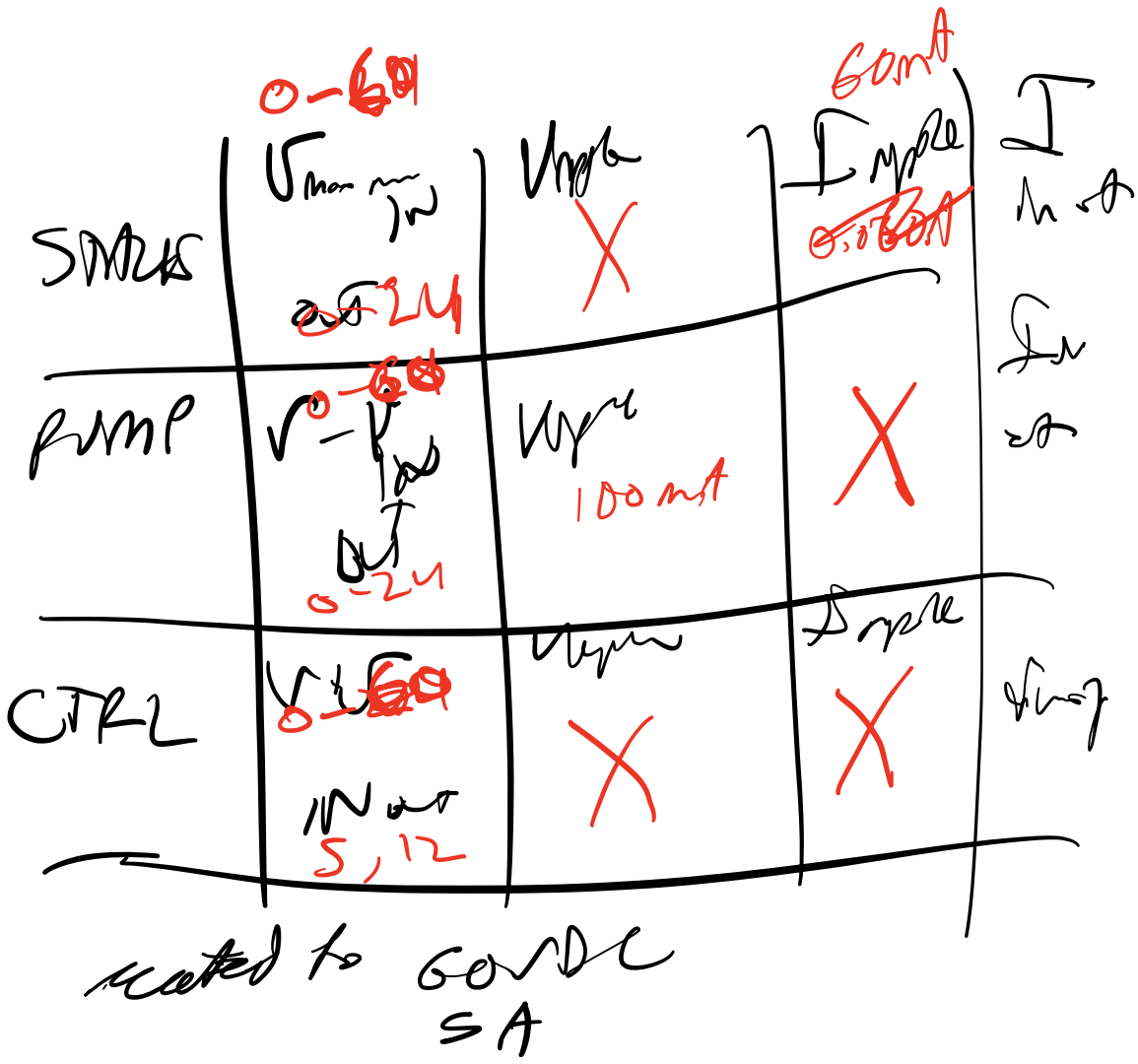
- 24V DC (nominally) pump w/ ~ 12V–24V range
- max current = 0.9A ~26Ω
- ΔV_{ripple} = ~~0.5V~~ 100mV

- variable voltage & current stocks
- Δi_{ripple} = 0.1A (based on factor of safety, i'lim)

from Melissa → 25 for this supply...
~ 0–30V range
~ 0–2A range
250mA
↓
ideally 10A for seawater

ΔV = 100mV
~30Ω
↓
L, C,
FET CURRENT RATING




SMPS
PUMP
CTRL
100 mA
5, 12
SA

BUCK SYNC'D P.S. CONVERTER SIZING

FET ✓ current good any in class work
diode ✓ current set ideally 460

let's choose L ... then C ...

CCM: $\frac{\Delta i}{2} \leq \langle i_L \rangle$ $\qquad V_L = L \frac{\Delta i}{\Delta t}$

$\langle i_L \rangle = \langle i_o \rangle$
bulk

$$L \geq \frac{V_L \Delta t}{2\langle i_o \rangle} = \frac{V_o (1-D) T}{2 \langle i_o \rangle}$$

D, $\langle i_o \rangle$ during worst times ...

L largest when $\langle i_o \rangle$ smallest ← 100mA ~

D smallest ... = 0

T choose $\frac{1}{30kHz}$ for familiarity ...

V_o largest = 30V

$L = 5\,mH$ $\qquad T = \frac{1}{30{,}000}$

$L = 1.5\,mH$ $\qquad T = \frac{1}{100{,}000}$

from ilim @ lowest conc. @ lin velocity
~ 200 rpm
~ 2 cm/s

$\Delta V = \frac{1}{8} \Delta i \, T \frac{1}{C}$ $\qquad$ from $q = \frac{1}{2} \langle i_{out} \rangle \frac{T}{2}$

$\Delta i/2$

$$C \geq \frac{1}{8}\,\Delta i\,\frac{T}{\Delta v}$$

$\Delta i \cong 2\langle i_2 \rangle \cong 2\langle i_0 \rangle$
$\cong 2(.1\,A)$
min
i.output

$C \geq \frac{1}{8}(0.2A)\frac{\left(\frac{1}{100{,}000}\right)}{0.1\,v}$ ← min f, ← min ripple

$\Delta i \cong .2A$

w/ max current :- 3A, 5A

$\Delta V_{spec} \sim 100\,mV \sim 0.1\,V$

$C \geq 2.5\mu F$ @ up to 60V to be safe...

if $T = 30{,}000$ @ $\Delta i \cong 200\,mA$ and $\Delta v \sim 50\,mV$

$C \geq 17\mu F$ capacitance not an issue...

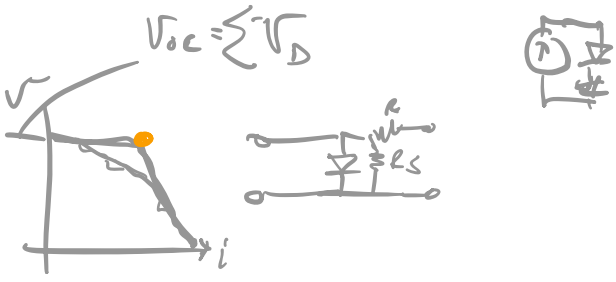
if $C \sim 1000\,\mu F$ (1mF) then ‖ 220μF → 0.011 V, 11mV

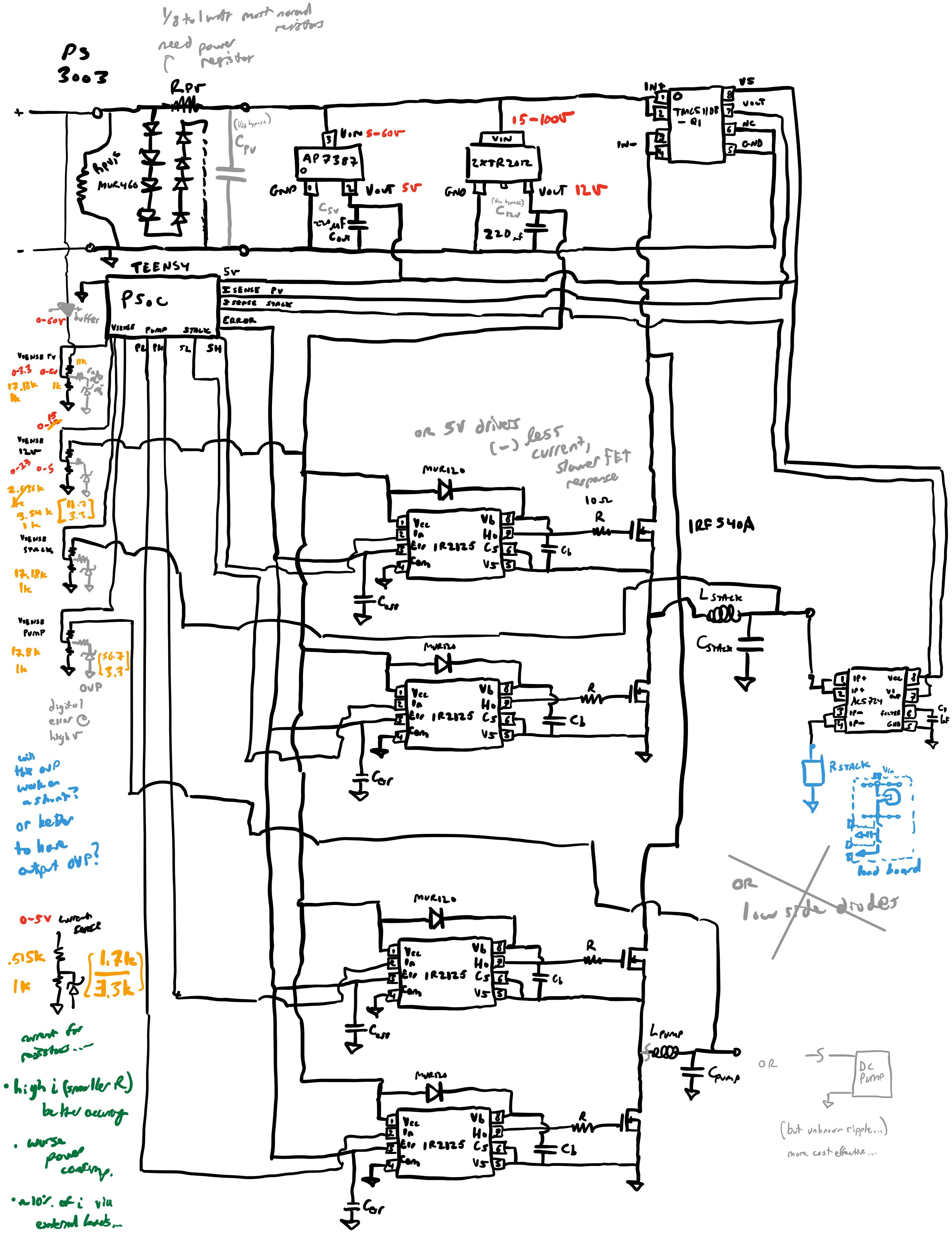
$$\Delta v \sim \frac{1}{8}(0.2A)\left(\frac{\frac{1}{10{,}000}}{1mF}\right)$$

$\sim 0.0025\,V$ $\sim 2mV$

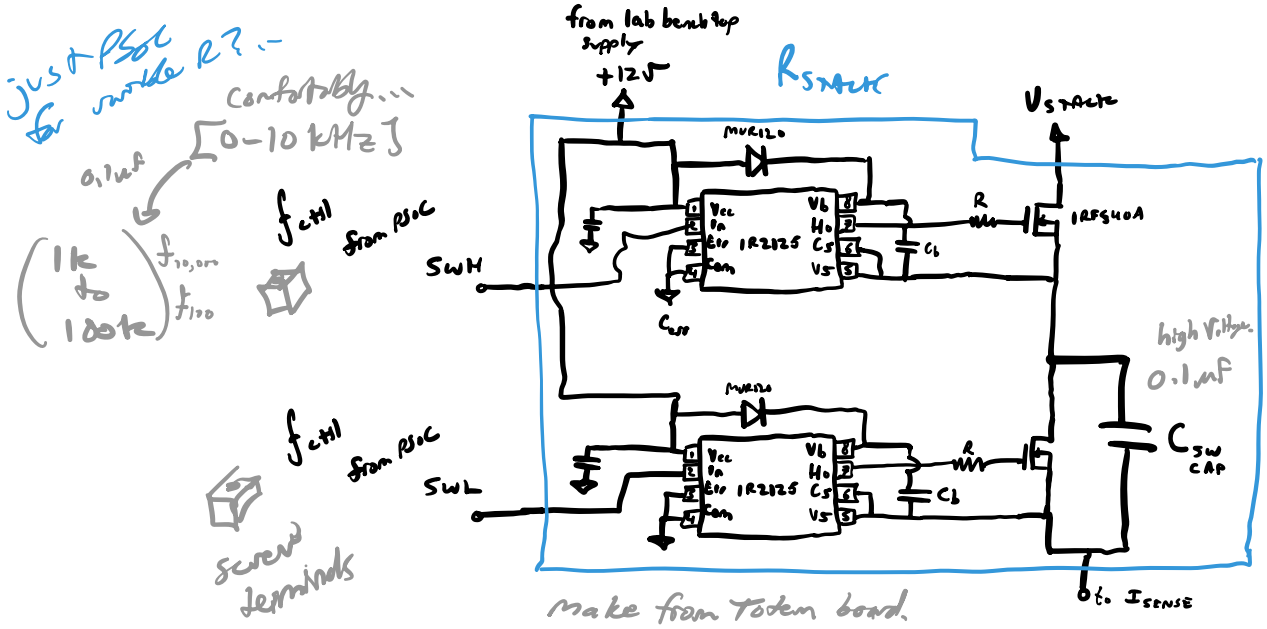
w/ 5A 10kHz 220μF → 0.284 V ripple

5A 10kHz 1000μF → 0.0625 V ripple



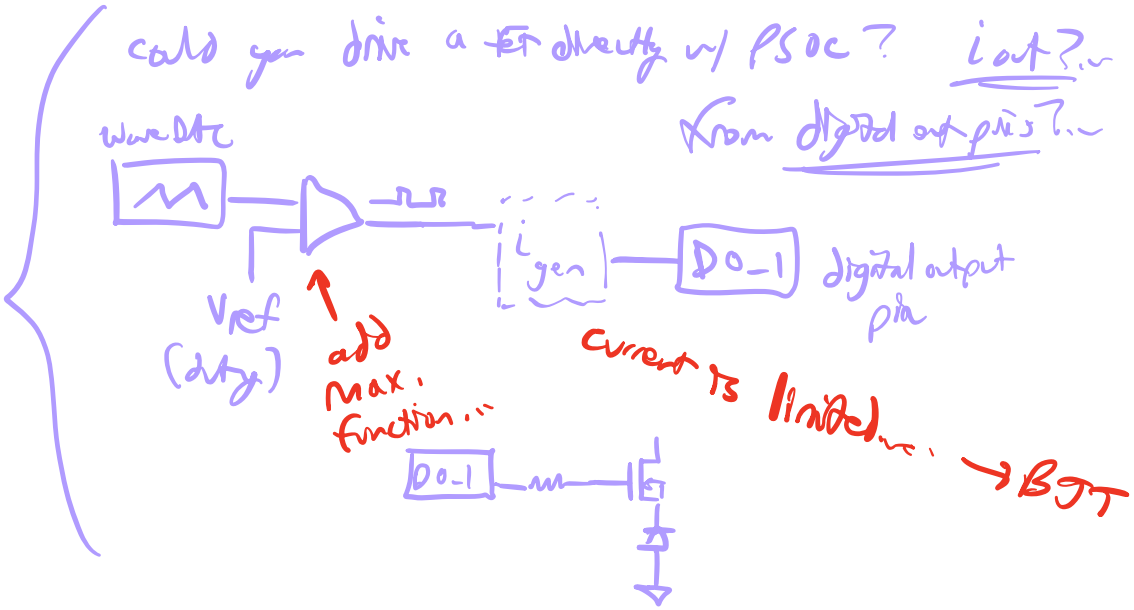


PS 3003
1/8 to 1 watt most normal resistors
need power resistor
RPV
MUR460
CPV
AP7387
VIN 5-60V
GND
VOUT 5V
CSV
COUT
ZXTR2012
15-100V
VIN
VOUT 12V
C12V
220 µF
TMCS1108 - Q1
VS
VOUT
NC
GND
TEENSY
PSoC
5V
ERROR
VSENSE
PUMP
STACK
PL
PH
SL
SH
buffer
0-60V
VSENSE PV
11k
VSENSE 12V
VSENSE STACK
17.18k
1k
VSENSE PUMP
12.8k
OVP
digital error @ high V
will the OVP work on a short?
or better to have output OVP?
0-5V current sense
.515k
1k
1.7k
3.3k
current for resistors...
• high i (smaller R) better accuracy
• worse power consumption
• ~10% of i via external loads...
or 5V drivers (-) less current, slower FET response
MUR120
IR2125
Vcc
In
Err
Com
Vb
Ho
Cs
Vs
10 Ω
R
Cb
IRF540A
CERR
LSTACK
CSTACK
ACS724
RSTACK
load board
OR
low side diodes
LPUMP
CPUMP
DC Pump
(but unknown ripple...)
more cost effective...



- PSoC ground unused DO pins (or assign them)

- digital output limited to ~0 or 5V 10kHz
- expected input PSoC digital ⎍⎍ 0 to
  analog ∿∿ 0 to ~~5V~~ 4V
  experimentally reliable (comparator)



- ways to visibility on PSoC? (scope) seems like impossible.
- explain drive modes (strong, high impedance etc) ✓
- analog input? ... where? ADC
- U sense & OVP
- general circuit review

- more analog inputs? (PSoC GPIO is analog, digital IO bidirectional.

try P0.7, P1.1, P1.2 w/ an analog input... (sampled to smooth...)

"P0" just artifact of CBZ ← check limitations

P0.7, P1.1 } optocoupled (likely not bidirectional)

P0.4, P3.2 } bypass caps warning.

Shunt Resistance (R_{sh}) and Series Resistance (R_s)

During operation, the efficiency of PV cells is reduced by the dissipation of power across internal resistances. These parasitic resistances can be demonstrated as a parallel shunt resistance (R_{sh}) and series resistance (R_s), as depicted below.

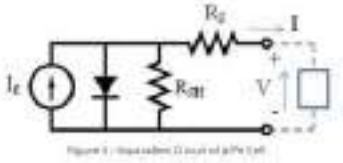


Figure 8. Equivalent Circuit of a PV Cell

Decreasing R_{sh} and increasing R_s will decrease the fill factor (FF) and P_{max} as shown in Figure 9 below. If R_{sh} is decreased too much, V_{oc} will drop, while increasing R_s excessively can cause I_{sc} to drop instead.

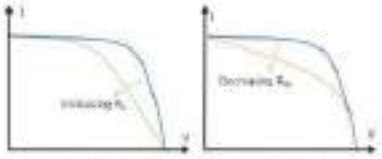
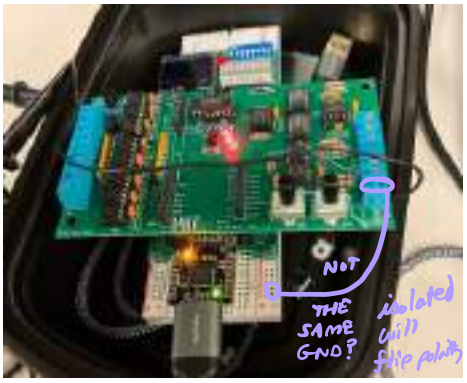
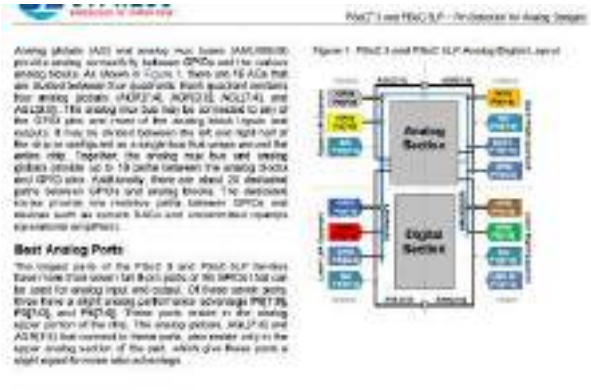


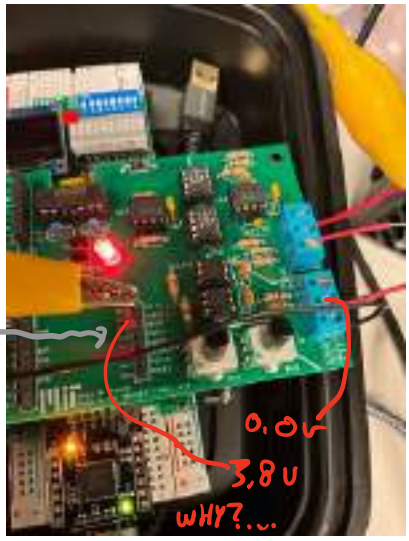
Figure 9. Effect of Changing R_s and R_{sh} from Ideality





- Digital Input pins pulled high 3,7, 3,8 V

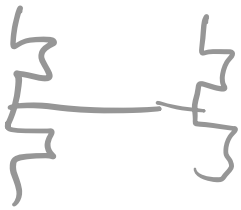
DI1, DI2 probed



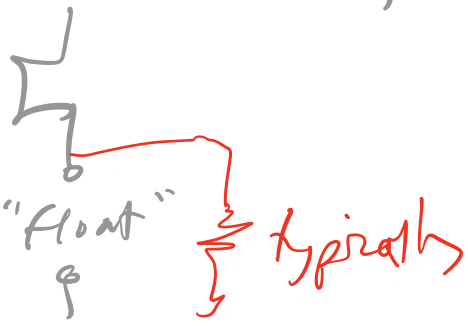
PS — pin signal
DS — into driver N, P FET } PIN to V high or GND

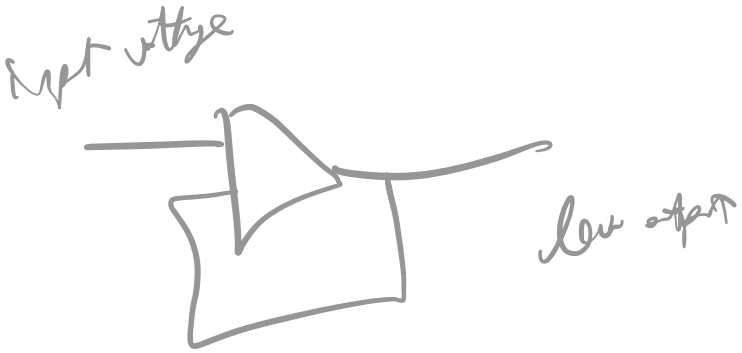
resistive pull-up: ⟶ asserts low, lets it go high

pull low



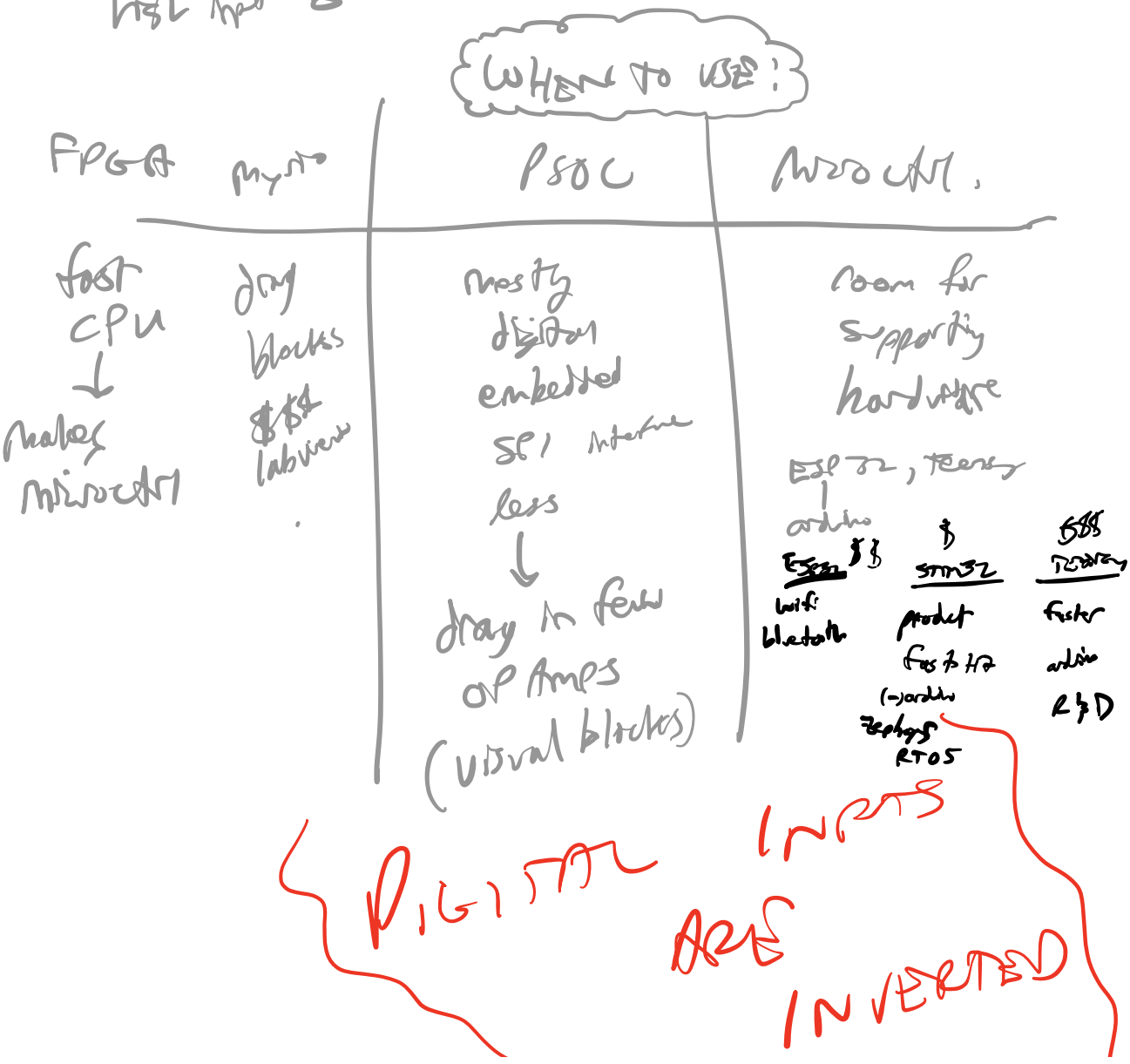
open source

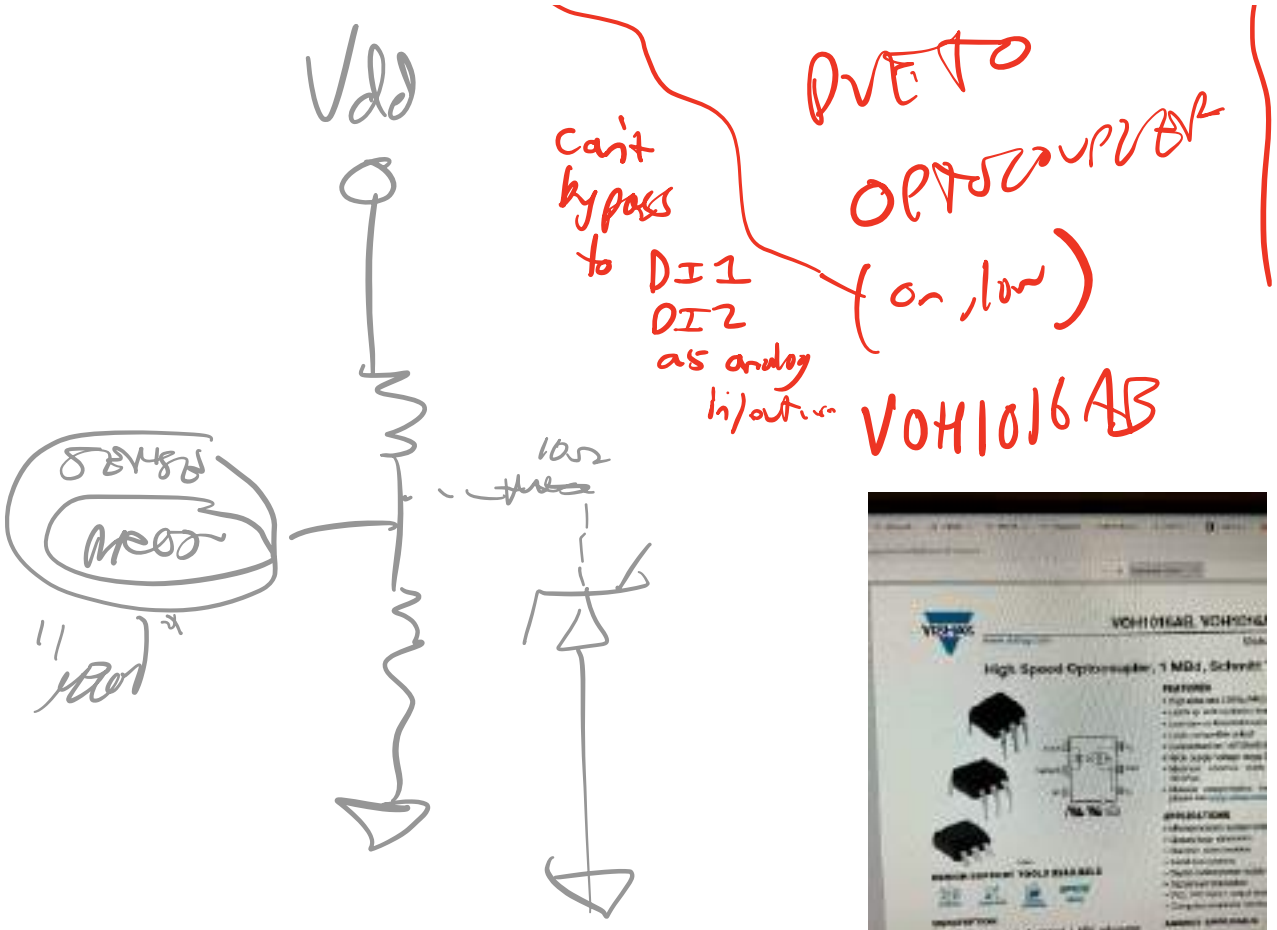




Buffer → upping current

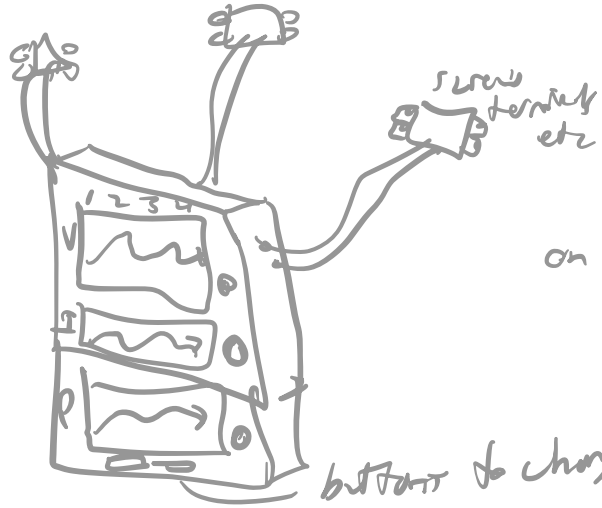
high input Z





IOEA "VIP" box ⇒ For transient response troubleshooting!!!

need to high current — has ROCP OVP OCP

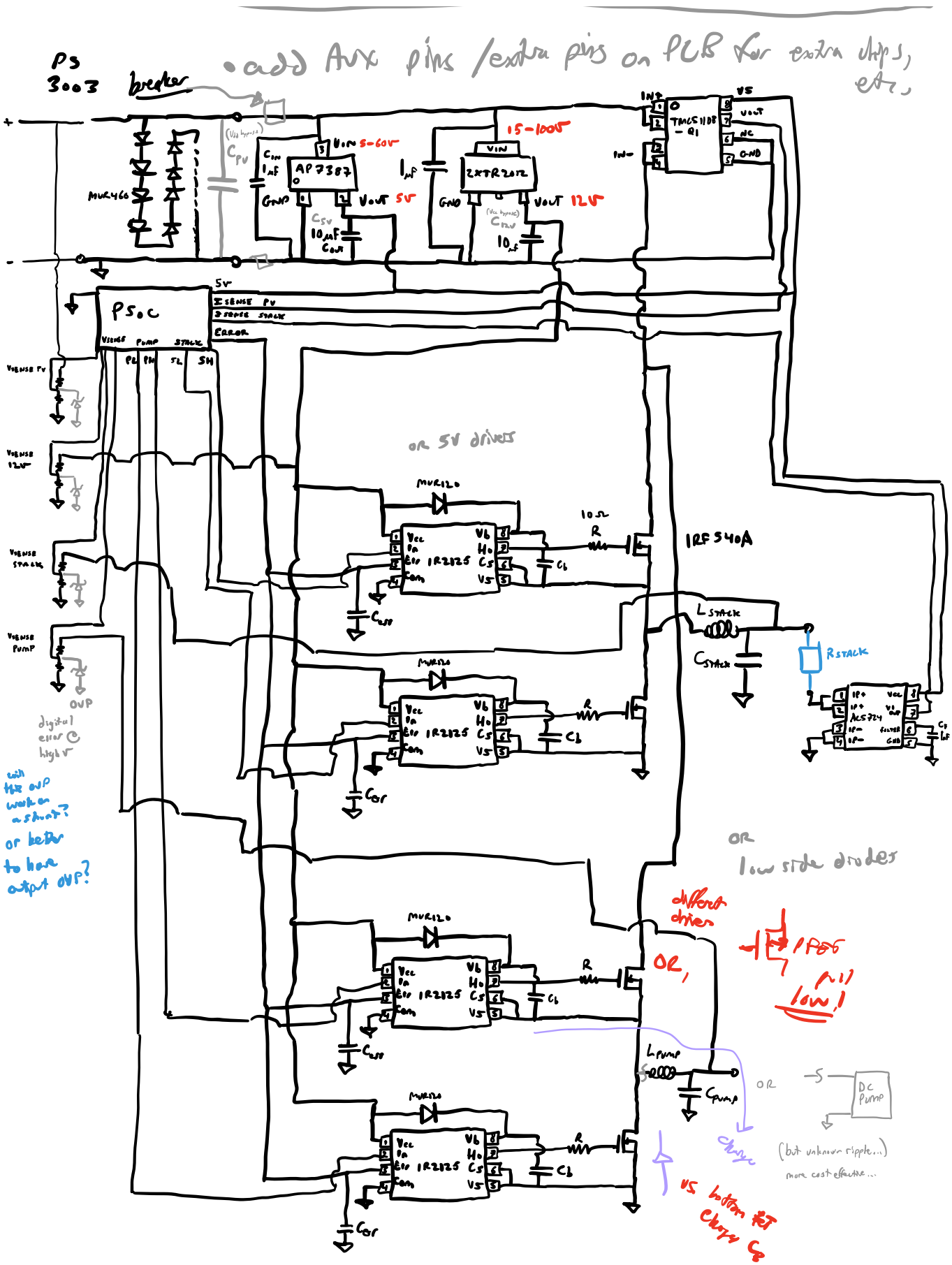


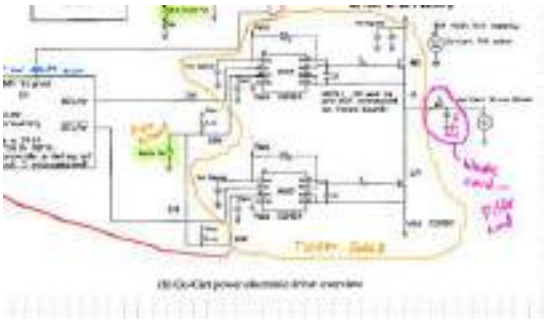
on off for 1,2,3?

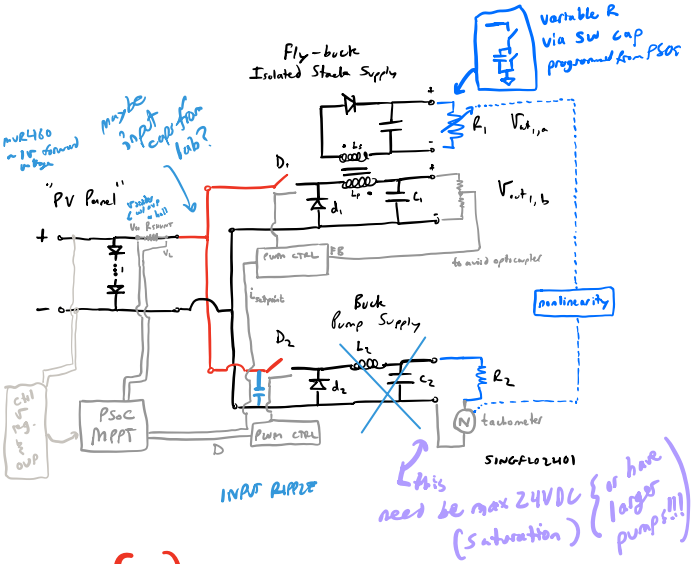
(seconds, minute) recording.

button to change time scale

(save function)


PS
3003
breaker
• add Aux pins / extra pins on PCB for extra chips, etc.
MUR460
AP7387
5-60V
5V
15-100V
2XTR2012
12V
TMCS1108 - Q1
PSoC
5V
SENSE PV
SENSE STACK
ERROR
VSENSE PV
VSENSE 12V
VSENSE STACK
VSENSE PUMP
OVP
digital error @ high V
will the OVP work on a short?
or better to have output OVP?
OR 5V drivers
MUR120
IR2125
10Ω
R
IRF540A
LSTACK
CSTACK
RSTACK
ACS724
OR
low side drivers
different drivers
OR,
IPB65
all low!
LPUMP
CPUMP
OR
DC Pump
(but unknown ripple...)
more cost effective...
VS bottom FET charge Cb





high side N
vs
low side P MOSFET

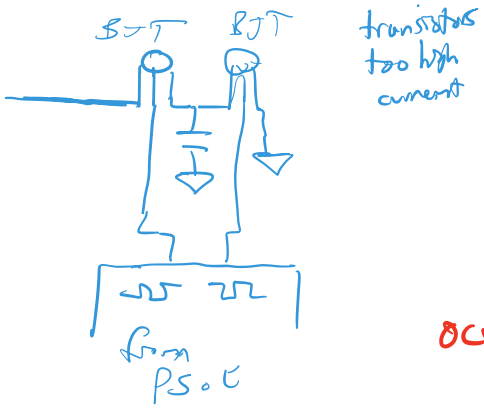
synchronous (low side FET) — (+) ΔV low side mosfet less than across diode.
asynchronous (power diode)

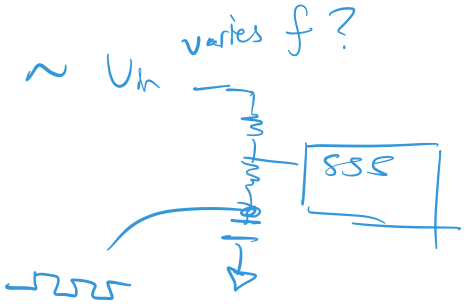
less power diss.
higher efficiency

↳ • reverse voltage
• forward voltage drop
• forward current
→ power dissipation

→ PFET (but must work if $V_{DD} < V_{LC}$)
→ need low side FET for C_b charge

or (high current!!!)





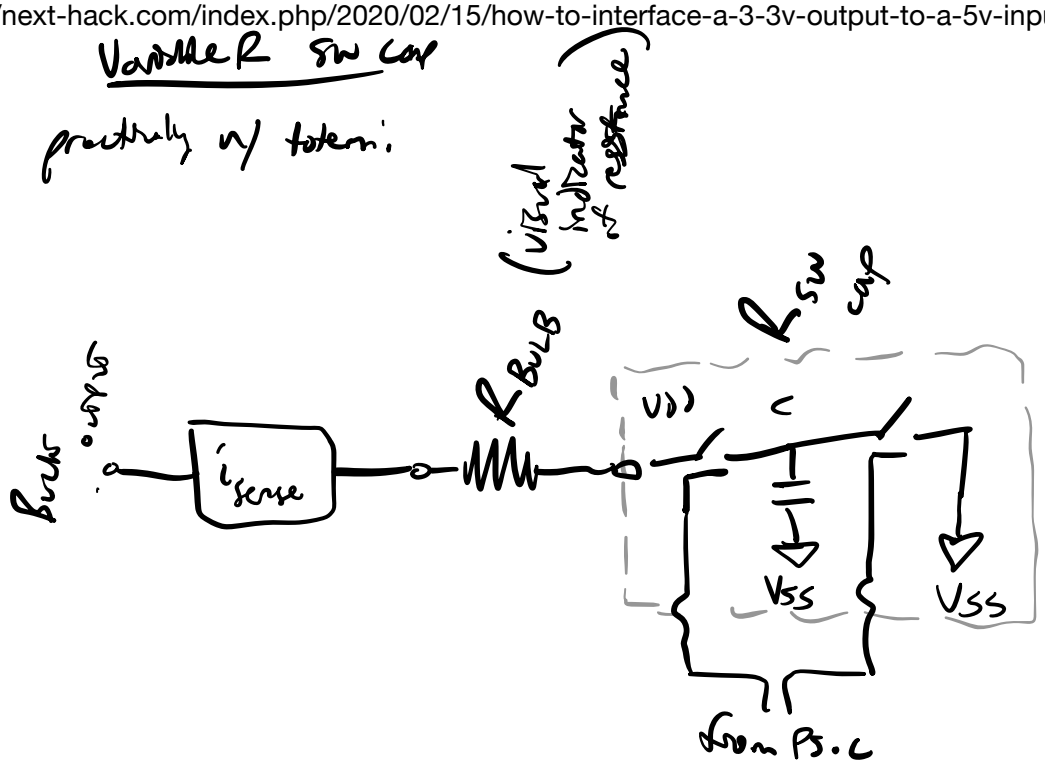
octo coupler typically digital

analog — non linear ...

https://next-hack.com/index.php/2020/02/15/how-to-interface-a-3-3v-output-to-a-5v-input/

Variable R SW Cap

practically w/ totem:



Analog in → variable clock PWM → digital out (to fans)

TODO:
- schematic for SW CAP VAR R
- PCB for SW CAP VAR R
- PSOC analog pin → clock troubleshoot in C code
  see clock "Set Frequency Example"

SELF - START CIRCUITRY

FOR CONTROLS

- switched cap.?

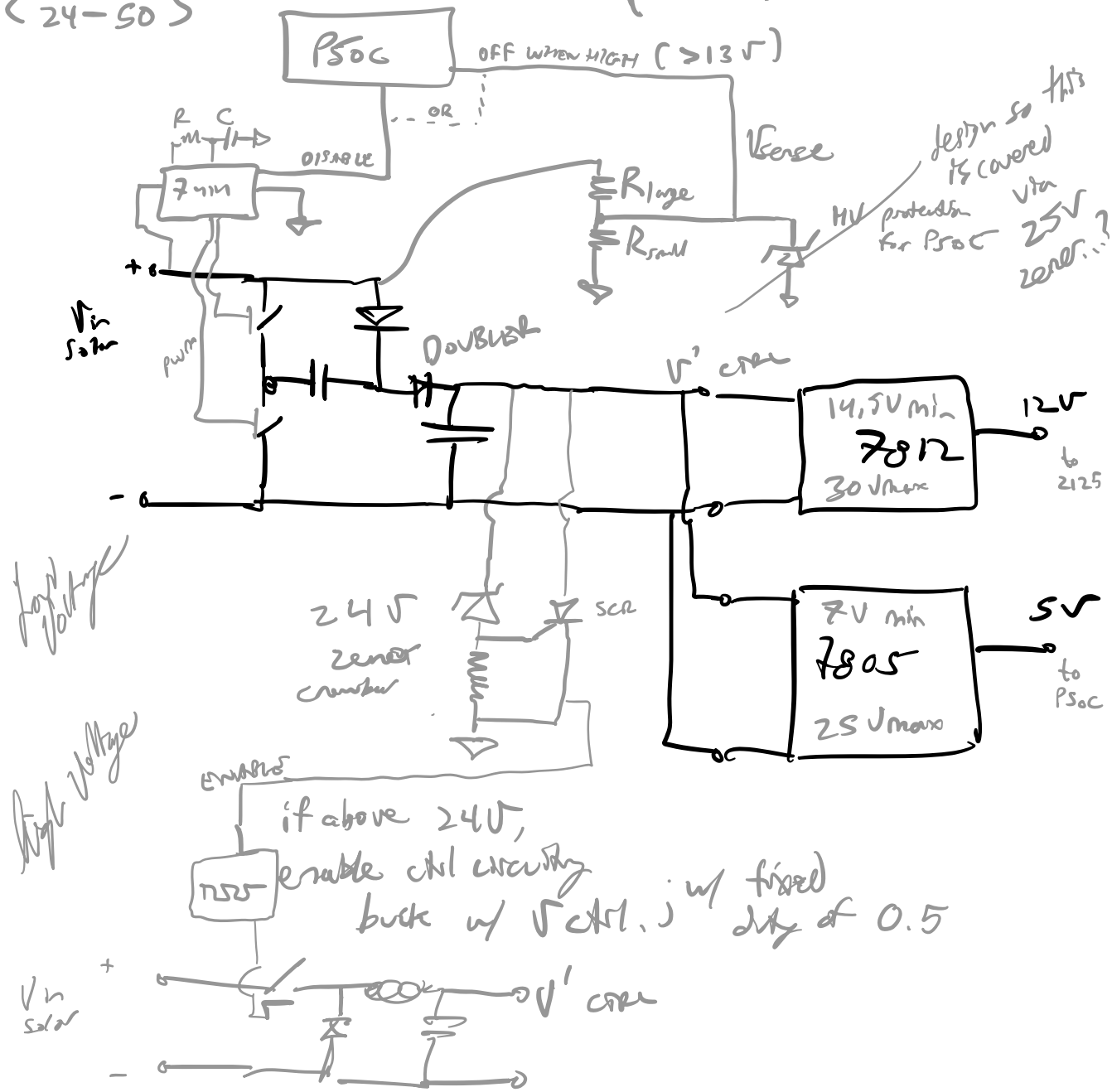
PSoC SLP

3.8 Boost converter internal — 3.3V 5V
0.5V min 5.5V max

doubler (for startup of drivers?)
12V 2125?

{0-13
13-24
24-50}

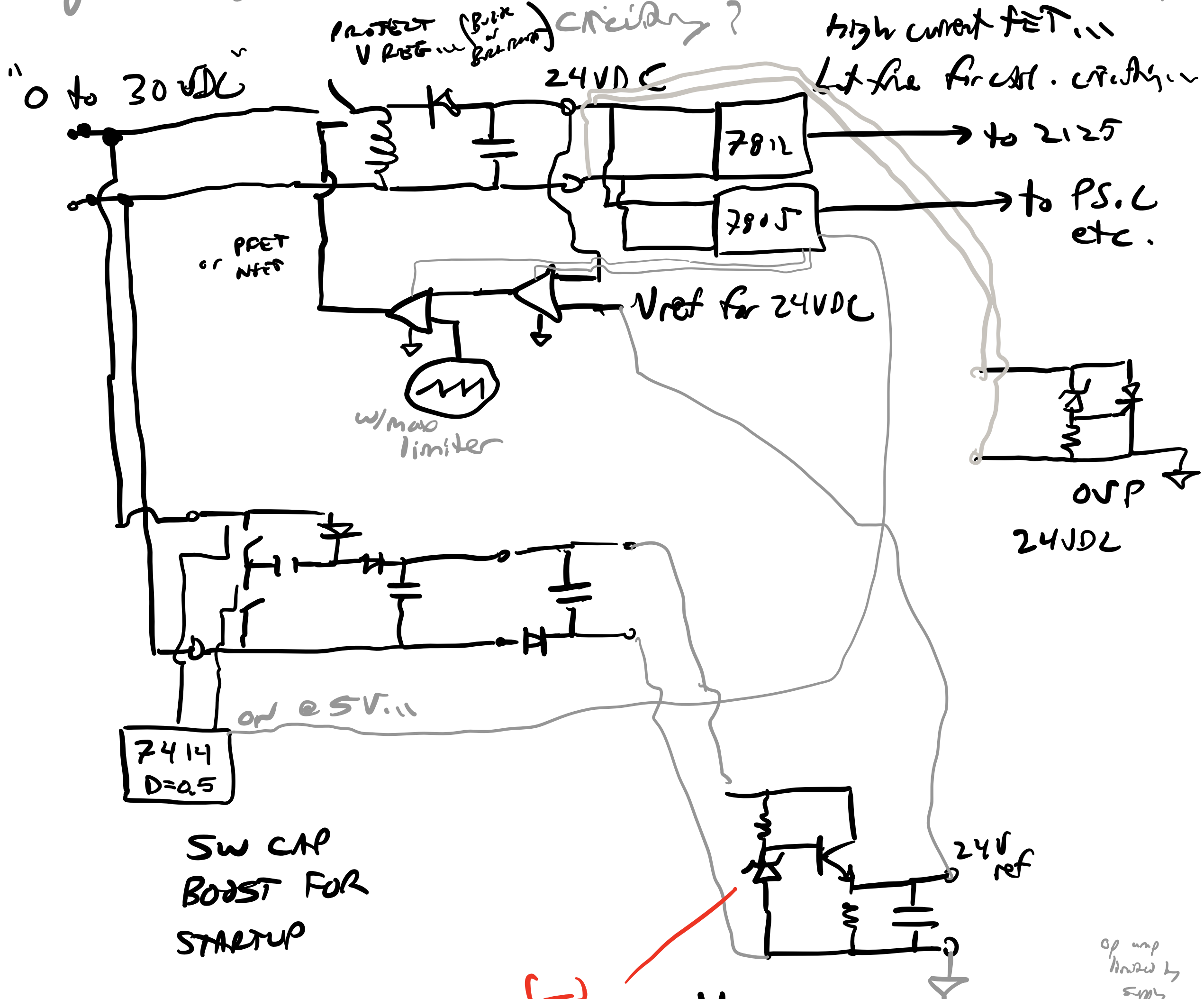
(when off, $V_{in\ solar} = V'$)



(1) PSoC on → PWM on → SW cap on from PV
↓
PV high ← lin. regulator to 12V for 2125
↓
SW cap off, PWM off
↓
2125 powered from PV panel

BUCK BOOST CTRL. CIRCUITRY POWER SUPPLY

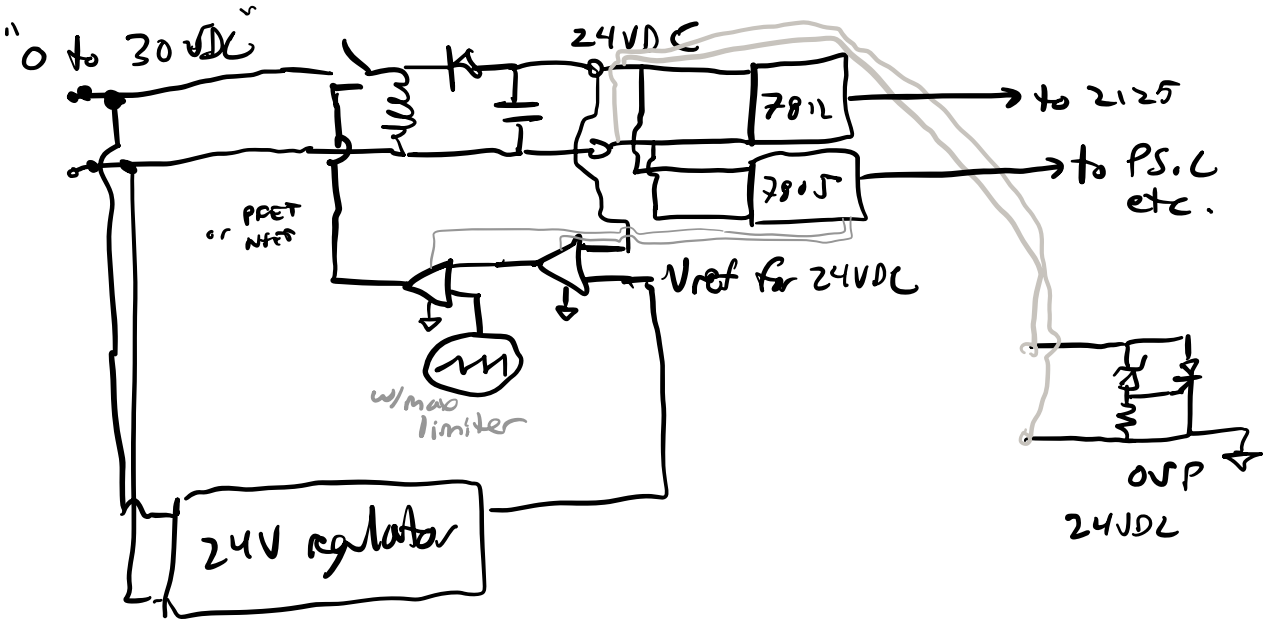
Why not just controllable buck-boost for ctrl startup circuitry?



(—) Max i(V applied) before breaks... Max back biased voltage

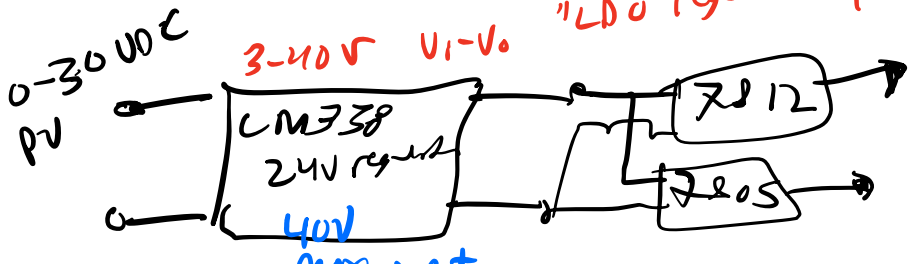
Vref regulator

op amp limited by supply rail...
or...
just let turn on when 7V min...?



e.g. LM338 ... but then why not...

"LDO regulators" (supply close to output)

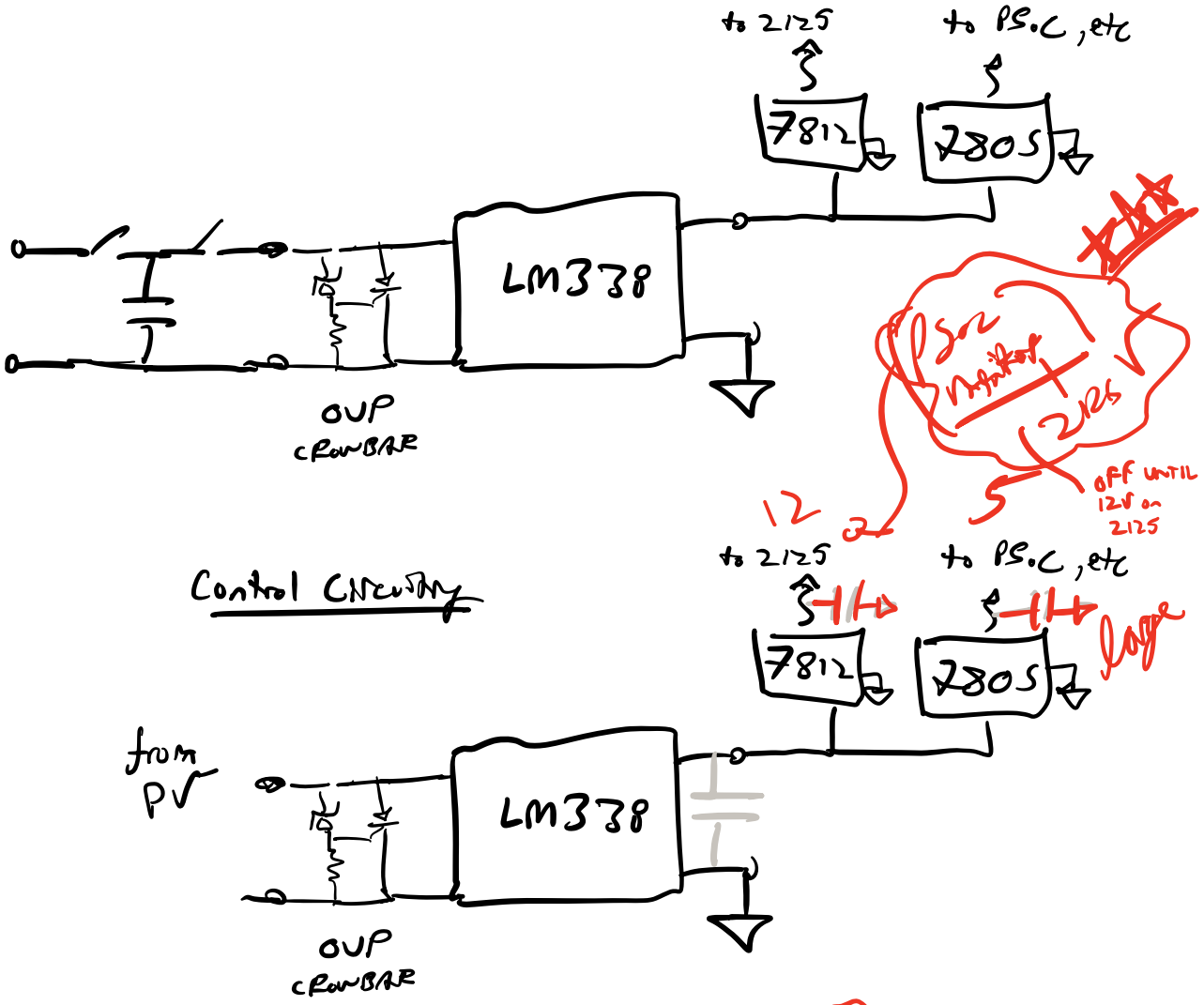


there exist linear regulators up to 450V input w/ 5V output...

op amp known by supply rail... or... just let turn on when 7V min...?

maybe can't handle high V?- ↓I?-

for ctrl. circuitry?...



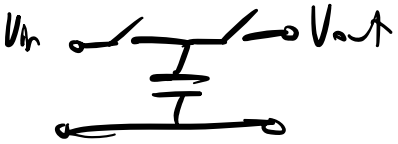
[Power path, monitor OVP UVP]

60V components withstand (see if we

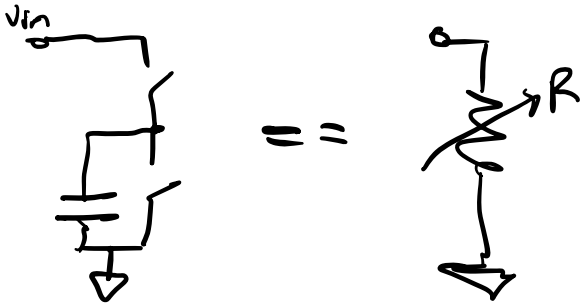
I can used sw. cap as a resistor programmable by f

$$R_{eq} = \frac{1}{C_s f}$$

↑ from PSoC

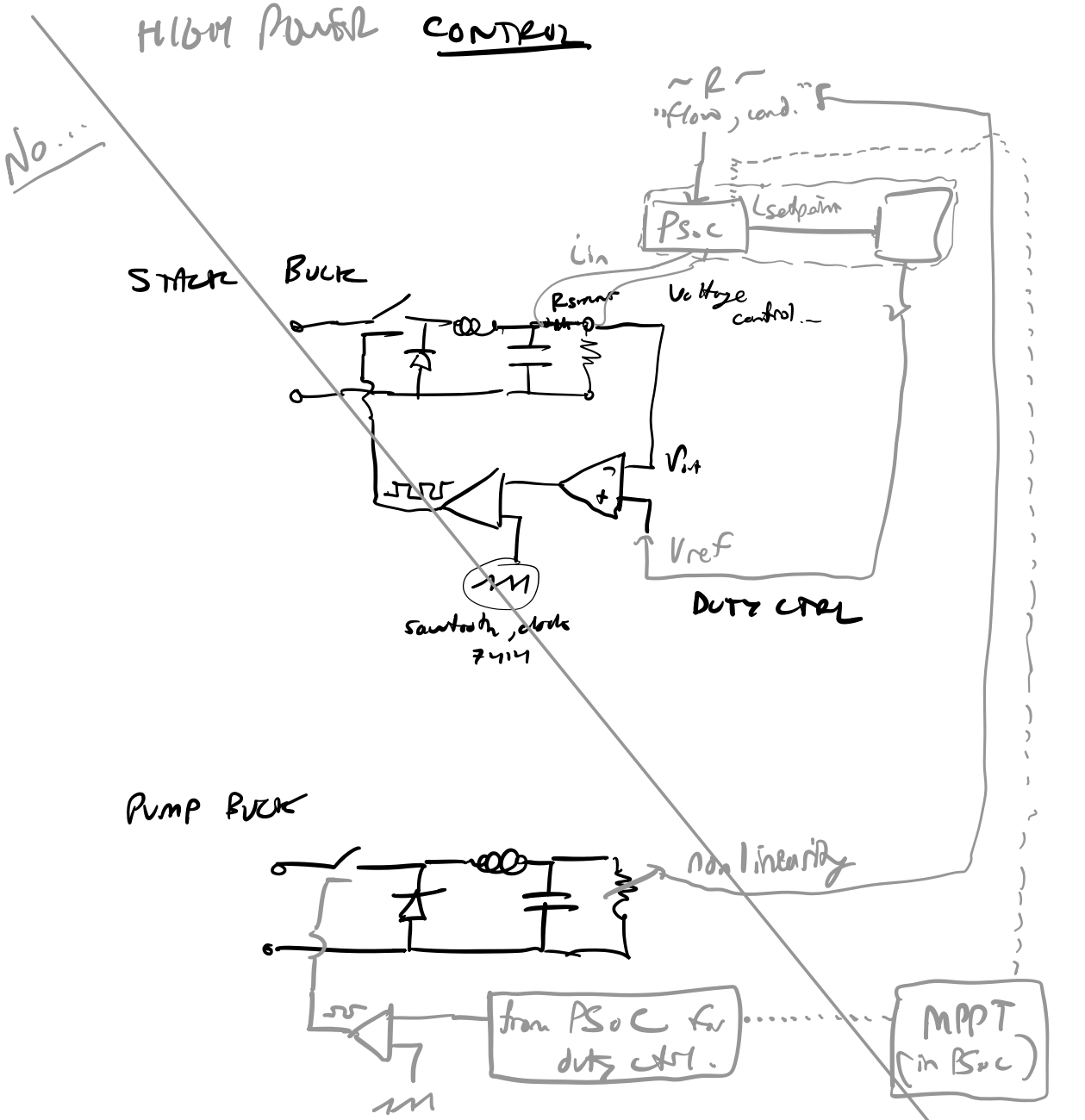


greater resolution

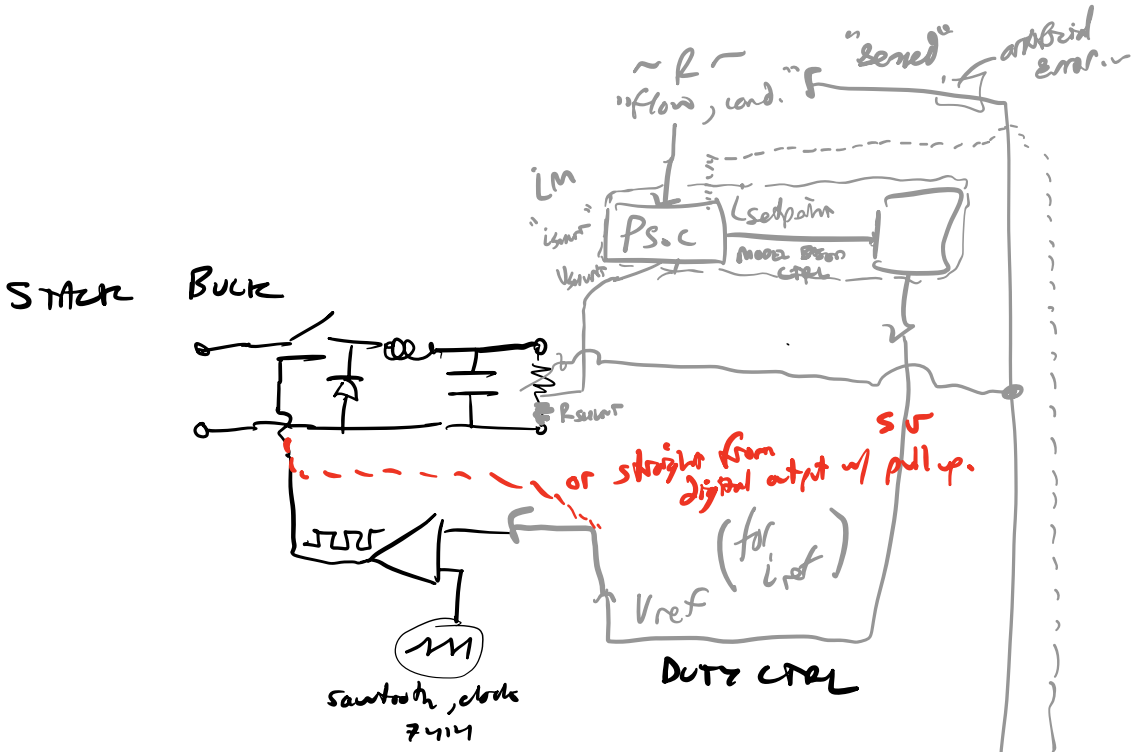


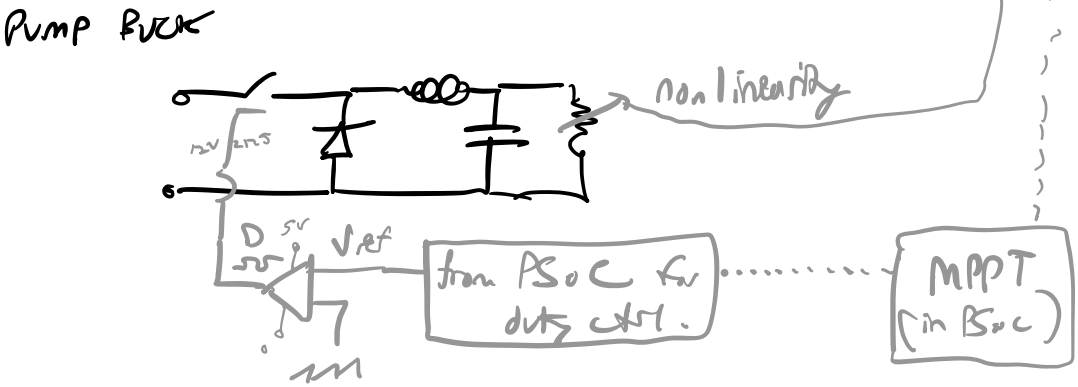
Which can simulate the electrodialysis stack!

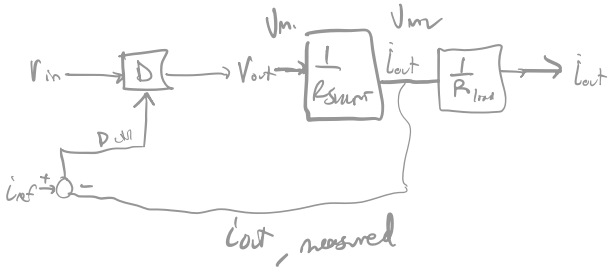
{ Chips 36V — 60V — 85V — 100V Si sizing }


HIGH POWER CONTROL
No...
"flow, cond."
PSoC
Lsetpoint
iin
STACK BUCK
Rsense
Voltage control
Vint
Vref
DUTY CTRL
sawtooth, clock 74114
PUMP BUCK
non linearity
from PSoC for duty ctrl.
MPPT (in PSoC)

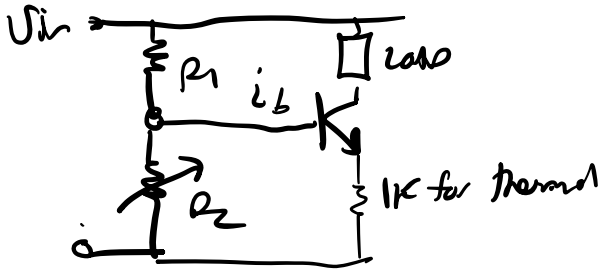
HIGH POWER CONTROL







§ Const. Current... b/c $i_e = (\beta+1) i_b$



$$I_L = \frac{V_b - 0.6}{R_e}$$ ← base voltage

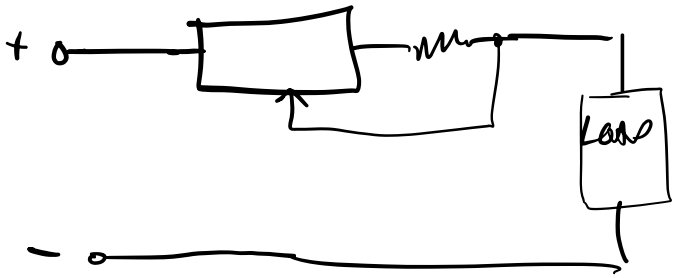
BJT → bad for thermal dissipation

Vary R_2 to ctrl current...

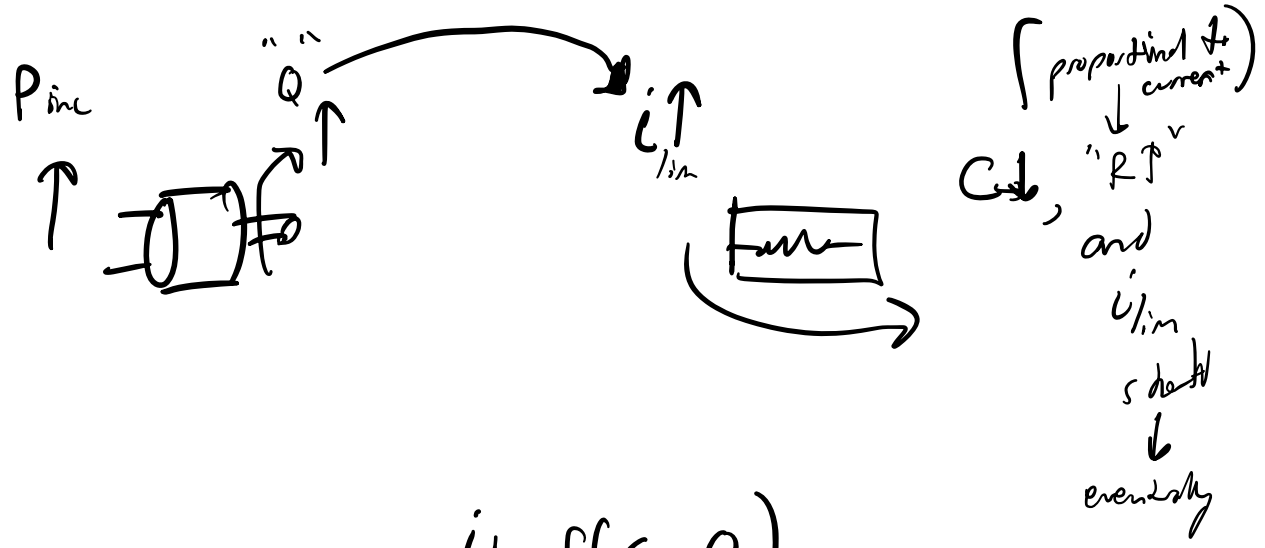
- const i → LED, batteries...

§ transient voltage suppressor diode 

§



§ Why not just duty control?...



$i_{lim}\ f(C, Q)$
$f(R, \omega)$
$f(R, v)$

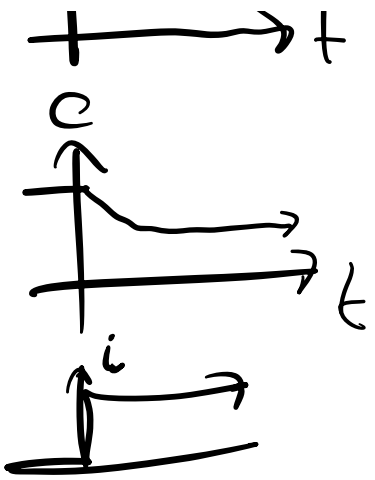
$Q\uparrow \longrightarrow \lim T \longrightarrow PT \longrightarrow \Delta C \downarrow$

(less resistance time -- but more current --)

$f(Q, C)$ or T ↓ until balanced

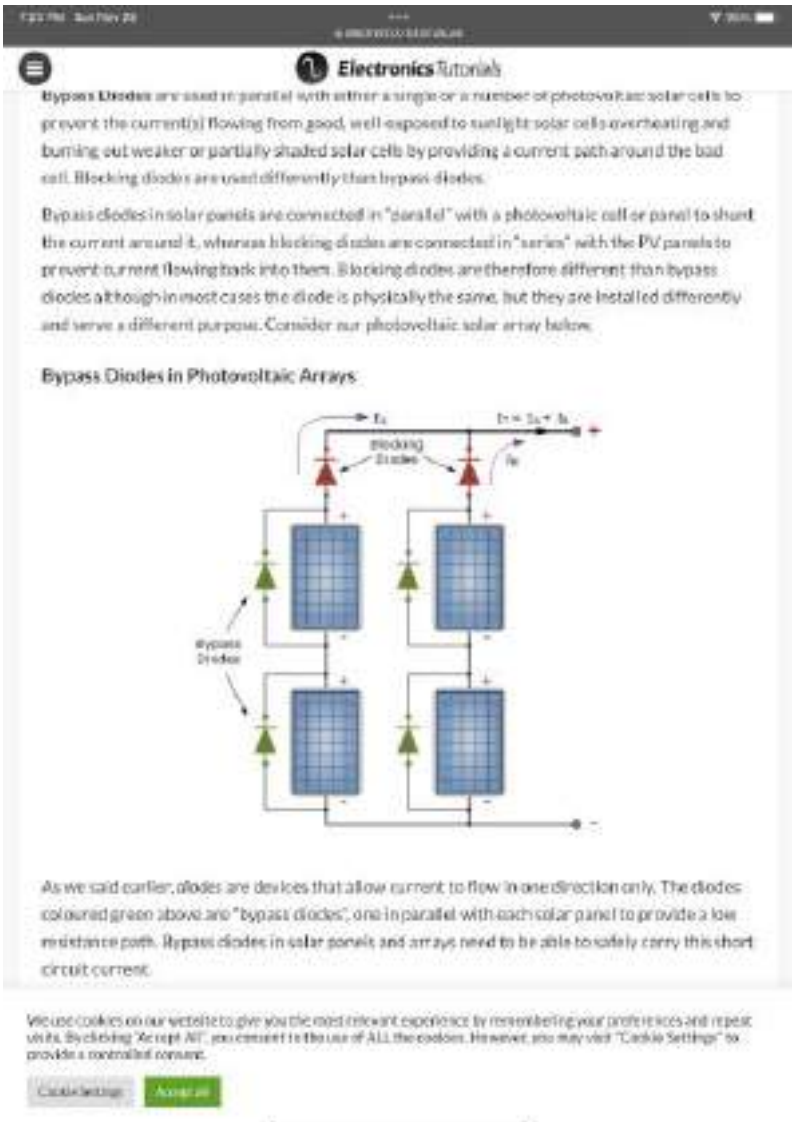
less res. T dominates, over current benefit... so C_{dil}, at some stability

R ↑ →



allowing more i flow,

but then at a certain point, i flow so high that C_{dl}, ext drops, balancing i flow. ∴



Electronics Tutorials

Bypass Diodes are used in parallel with either a single or a number of photovoltaic solar cells to prevent the current(s) flowing from good, well-exposed to sunlight solar cells overheating and burning out weaker or partially shaded solar cells by providing a current path around the bad cell. Blocking diodes are used differently than bypass diodes.

Bypass diodes in solar panels are connected in "parallel" with a photovoltaic cell or panel to shunt the current around it, whereas blocking diodes are connected in "series" with the PV panels to prevent current flowing back into them. Blocking diodes are therefore different than bypass diodes although in most cases the diode is physically the same, but they are installed differently and serve a different purpose. Consider our photovoltaic solar array below.

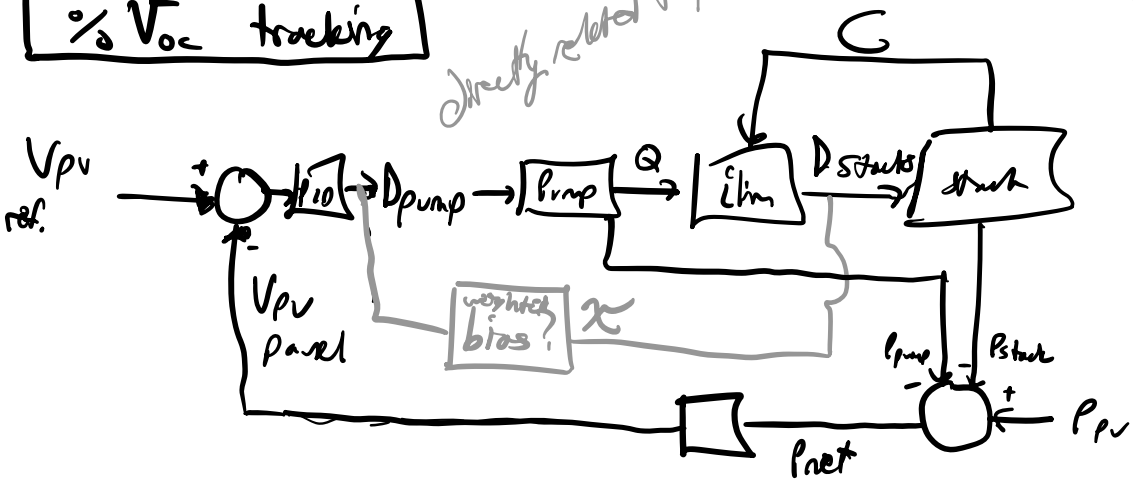
Bypass Diodes in Photovoltaic Arrays

As we said earlier, diodes are devices that allow current to flow in one direction only. The diodes coloured green above are "bypass diodes", one in parallel with each solar panel to provide a low resistance path. Bypass diodes in solar panels and arrays need to be able to safely carry this short circuit current.

Control

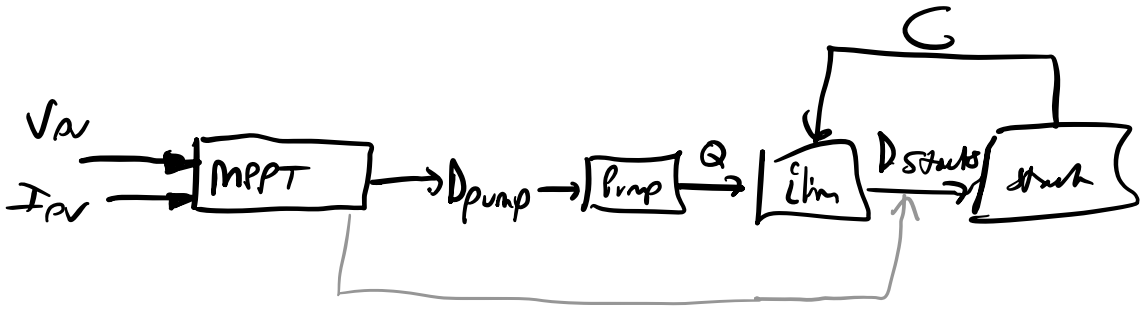
directly related to pump flow rate → predict i_{lim} & power & duty

% V_{oc} tracking



Perturb and observe

quick ramp down, slow ramp-up?
(more sensitive to over-than under shoot)



respond quickly for power down pmp threshold...

PV: 12–24 V typ

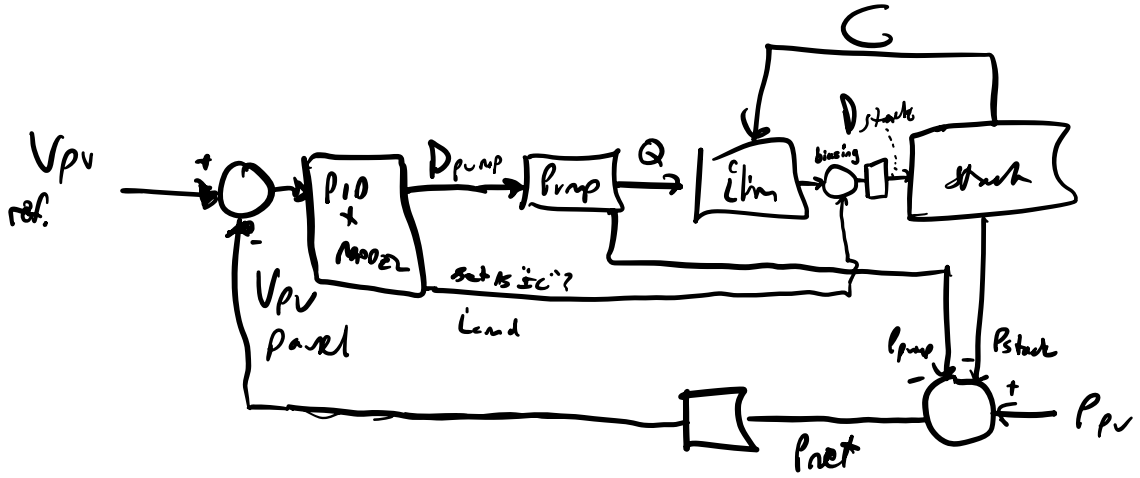
RULES / GUARD

nonlin: PSoC: — if driver V < 12 VDC
FETs command 0 DUTY
— if PV power drops rapidly
or threat to chip (< 15 VDC PV, OFF)

Control

% V_{oc} Tracking MODEL-INFORMED
INITIAL CONDITION

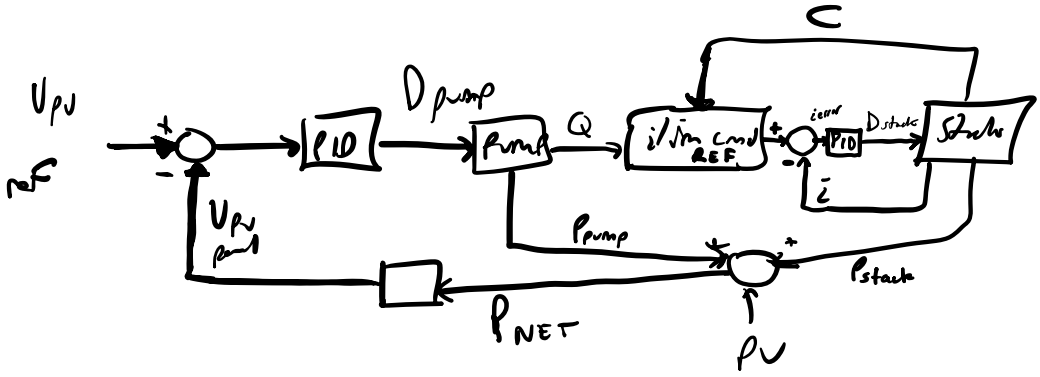
(eh...)



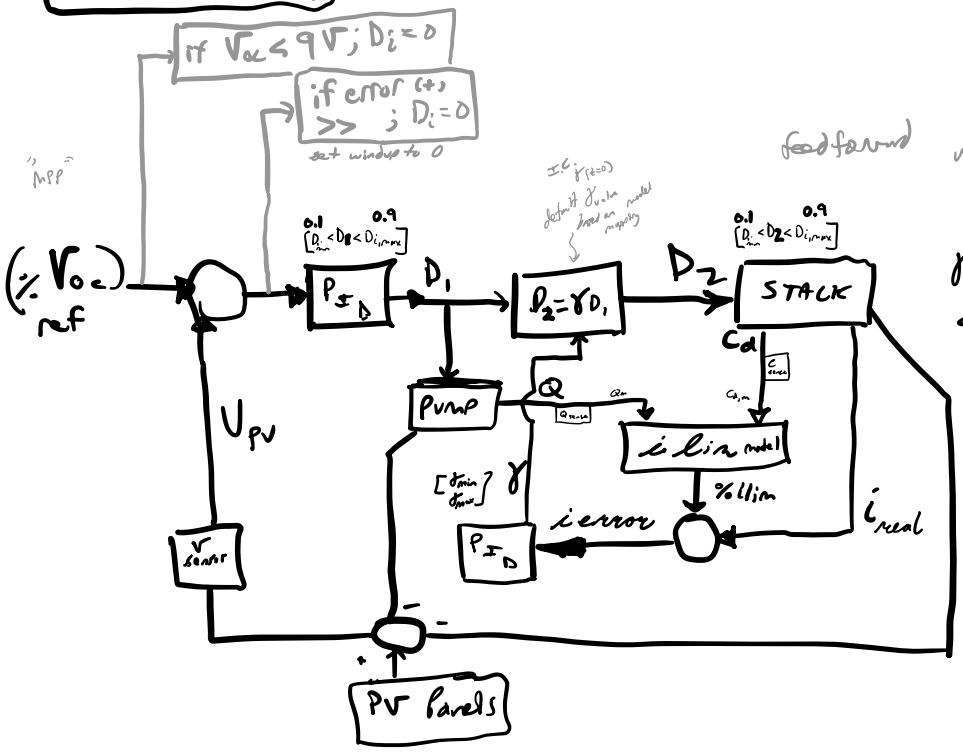
pre-empirical lookup table
directly related to pump flow rate ⟹ predict i_{lim} & power & duty

(closest to past)

% V_{oc} tracking CASCADE



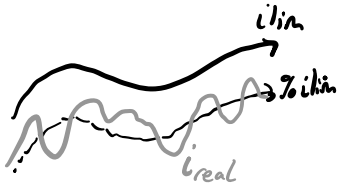
% V_{oc} Tracking CASCADE w/ LENIANCY (leniant)



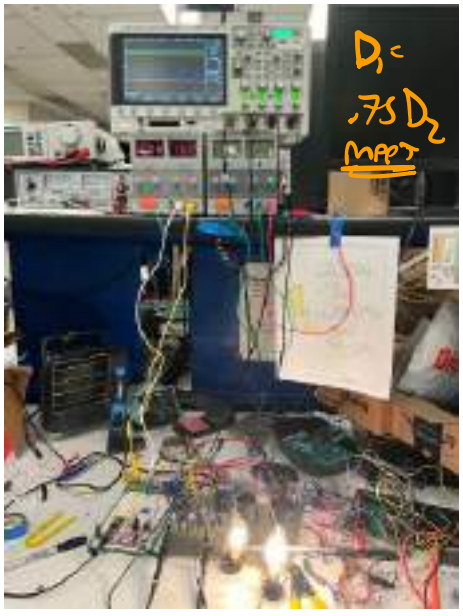
feedforward w/ buying from i_{lim}

γ changes based on i vs. i_{lim}

here, i need not be exactly i_{lim}

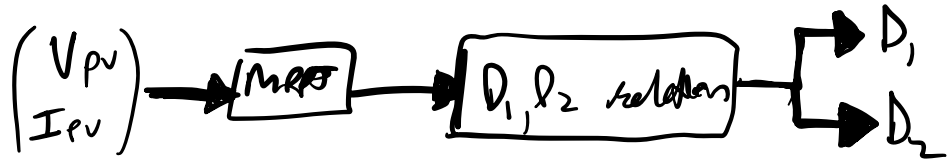


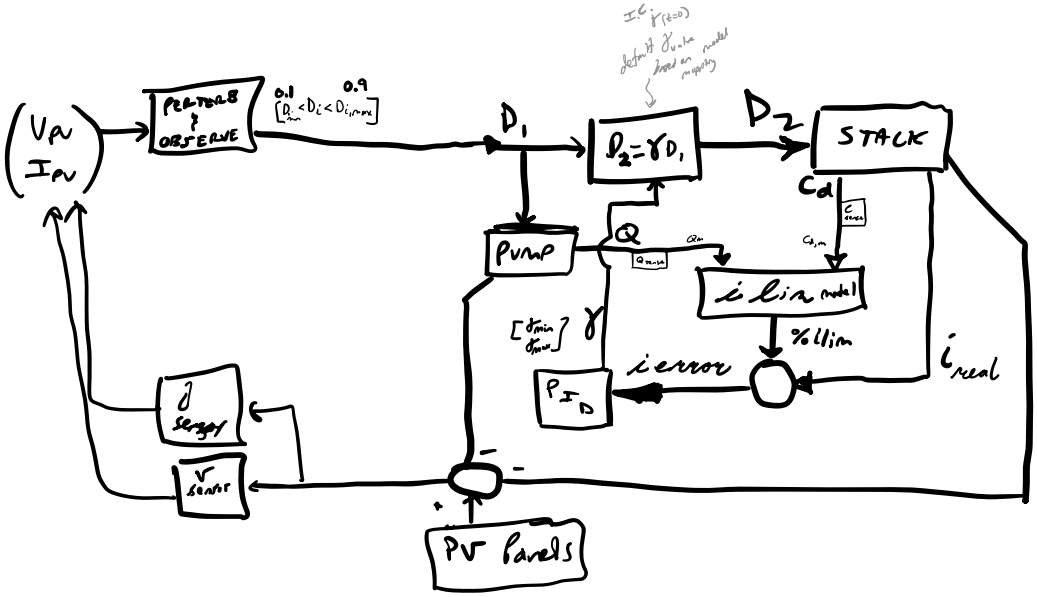
allows leniancy to avoid power overdraws



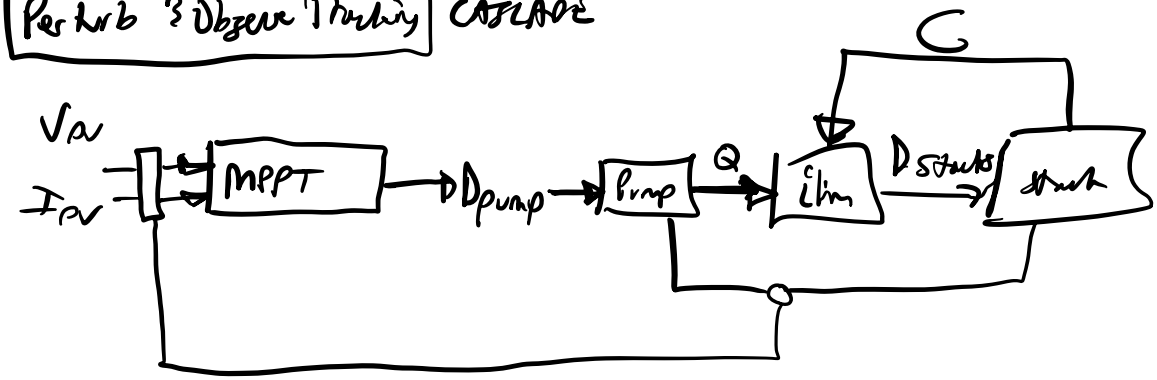
Perturb & Observe Method — General, 2 load

Two point power comparison method

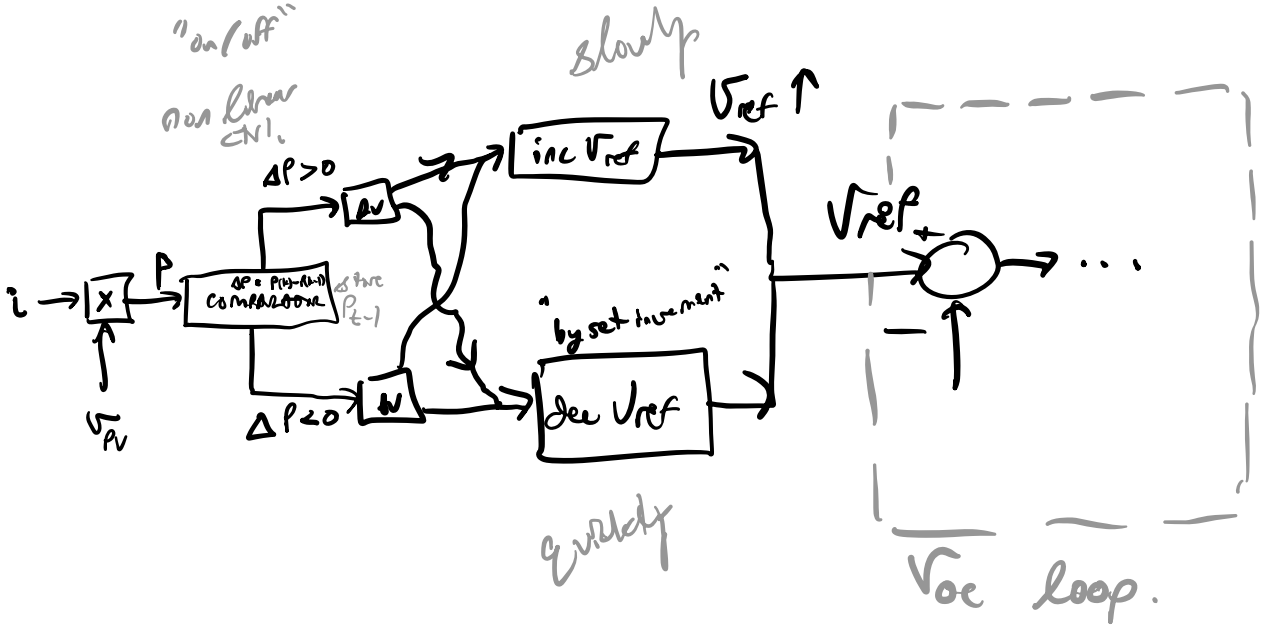


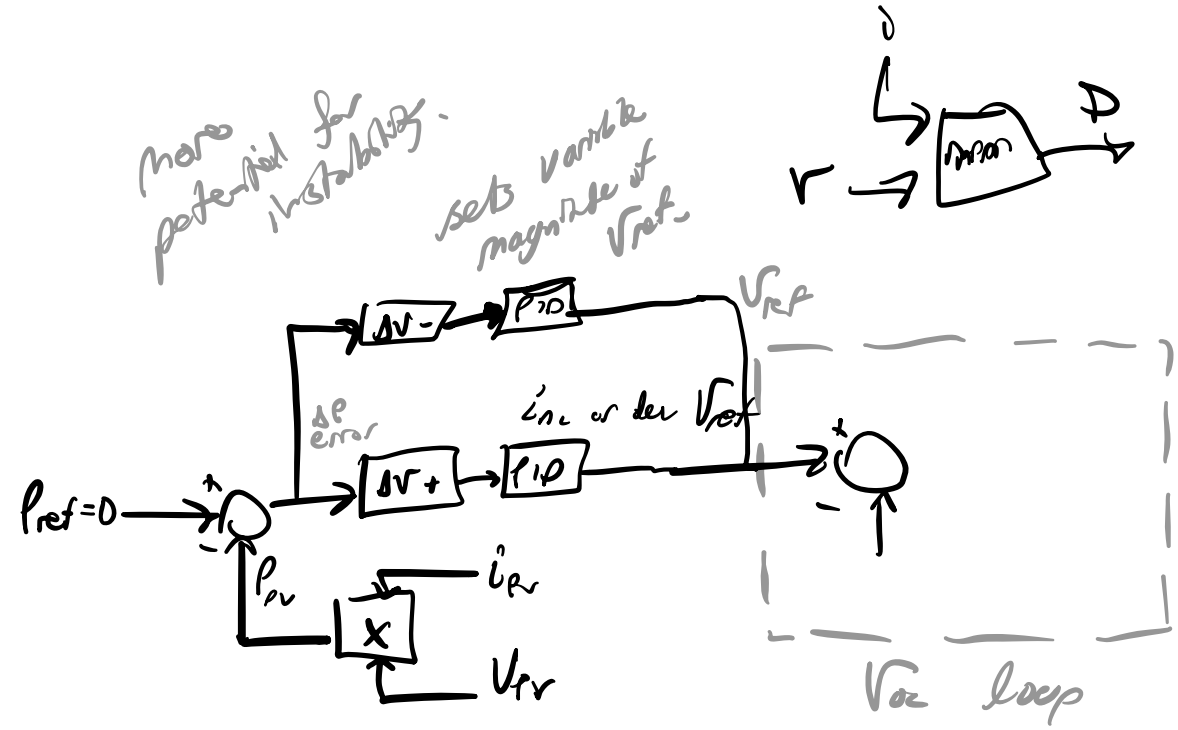


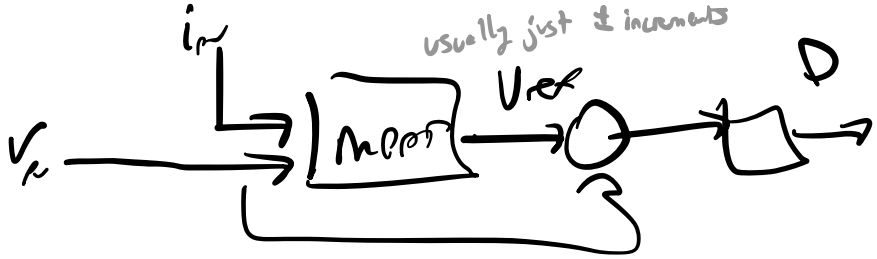
Perturb & Observe Method — CASCADE



PID } "Difficult to design"
SMC }

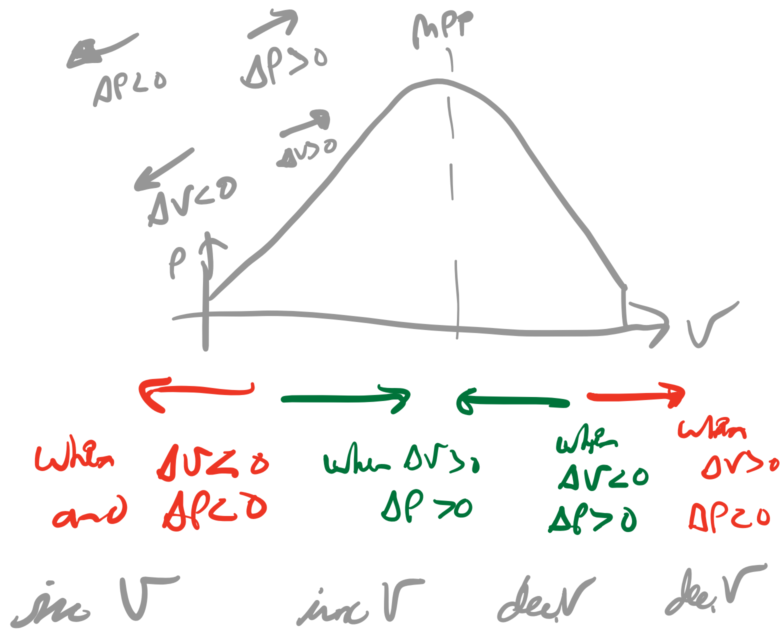

"on/off"
non linear ctrl.
slowly
$V_{ref}\uparrow$
inc V_{ref}
$\Delta P > 0$
ΔV
i
X
P
$\Delta P = P_{(t)} - P_{(t-1)}$
COMPARATOR
V_{PV}
$\Delta P < 0$
ΔV
dec V_{ref}
by set increment
V_{ref}
+
−
...
quickly
V_{oc} loop.


more potential for instability.
sets variable magnitude of V_{ref}.
i
V
P
V_{REF}
$\Delta V -$
PID
ΔP error
inc or dec V_{ref}
$\Delta V +$
PID
$P_{ref}=0$
+
−
P_{PV}
i_{PV}
X
V_{PV}
V_{oc} loop


i_{PV}
usually just ± increments
V_{PV}
V_{ref}
D

P&O

→ measurable dynamics



Limits / drawbacks

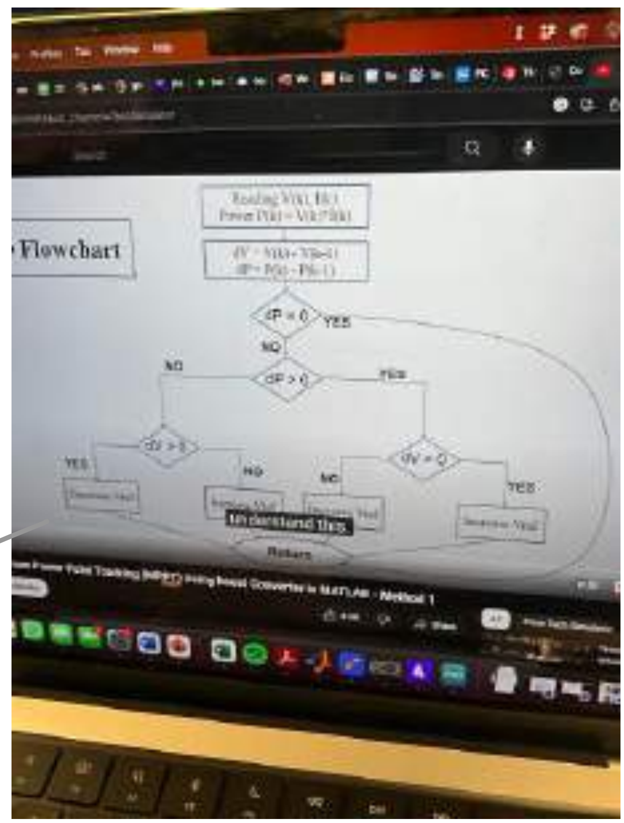
→ power oscillations

↔ perturbation step size...

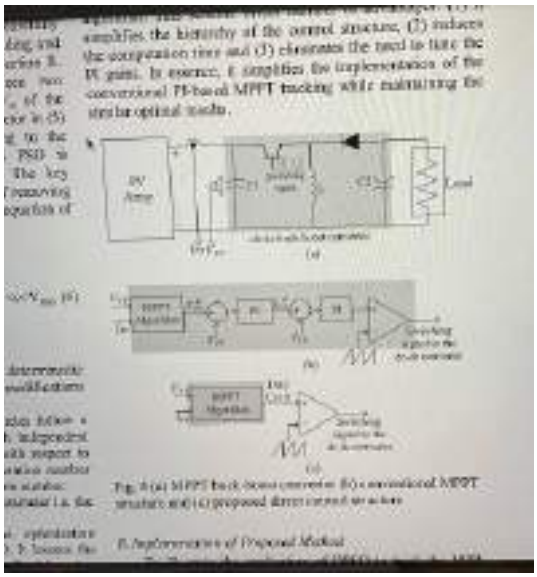
smaller reduces oscillations S.S.
BUT
bad PV trans. response

→ local min...

→ "drifting"

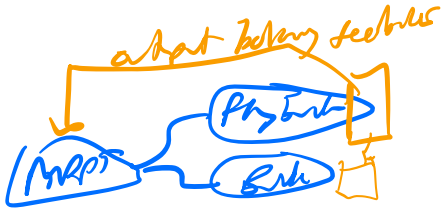


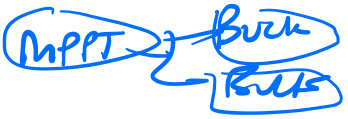
(since D dec D etc.)



Ishaque 2012
Salam

for TLD: CTRL arch
≠
IEEE Arch.





etc.

H bridge?

STEPS TO BUILDING

→ ½ Vdc w/ 1 Cap ✓ ; ½ Vdc w/ 2 caps ✓

→ P&O w/ 1 cap ; P&O ✗ w/ 2 caps ✗ need current sensing

P&O w/ ✓ 2 caps & biasing

IEEE Transactions on Power Electronics

12/6/23

→ clean up drawing

→ current sensors DIDN'T WORK

:(

→ MPPT 1 buck P&O algorithm......
2 buck

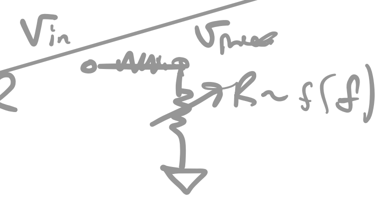
→ Lab: • i sensors? maybe there... → P.C. cell?
• pump, stack? → eventually...

→ fix BUCK 2 (problematic...)

{ideally P.C. cell hookup}

12/7/23

⇒ FIX & CHARACTERIZE PSoC var R



C	f	R

⇒ i sensor, P&O algorithm

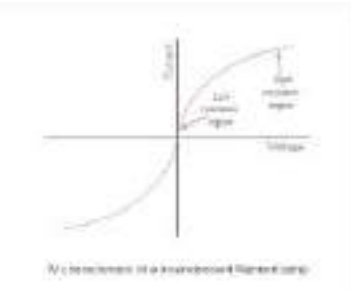
12/8/23

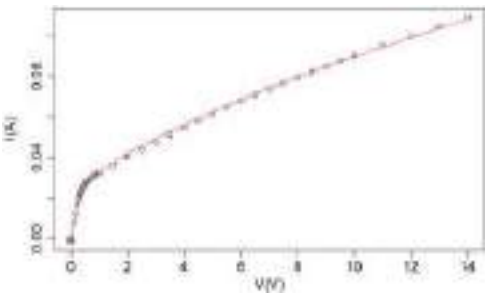
⇒ P&O alg. tuning params.
2 load P&O (lights vs. resistors?)

delay ? (PSoC) and/or main board

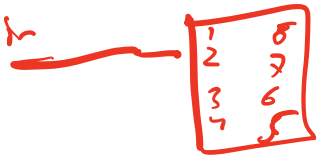
⟹ implement Rin current measurement function
↔ real sensor N, die, etc.
↔ 36,000 rpm ibin? depends on comp
(density agnostic of size...)

⇒ implement cond, Q sensing



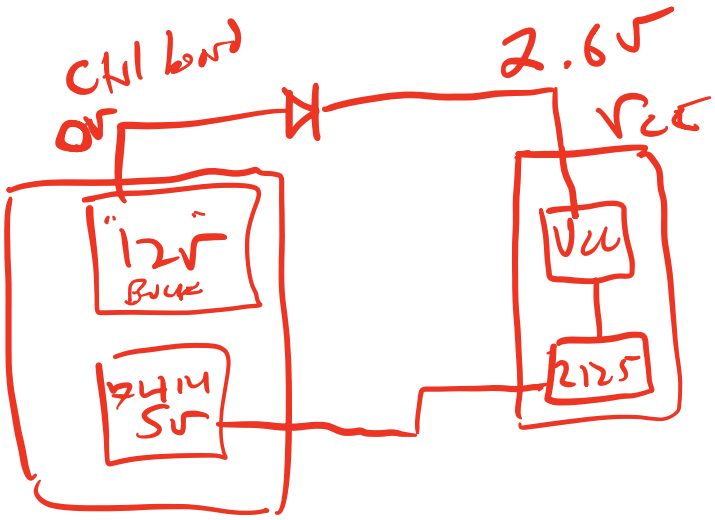


5V from 7414 ⟹ causing Vcc ½ 5V
~2.6V

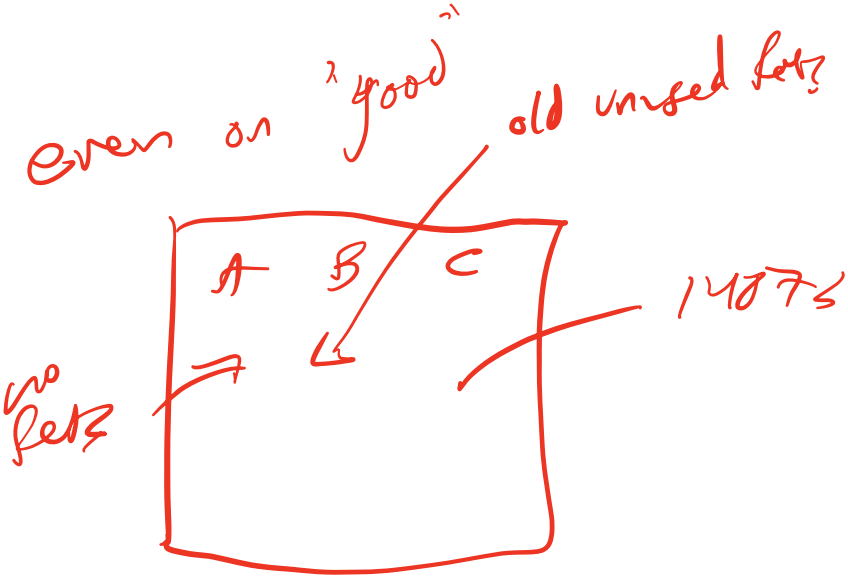
5V


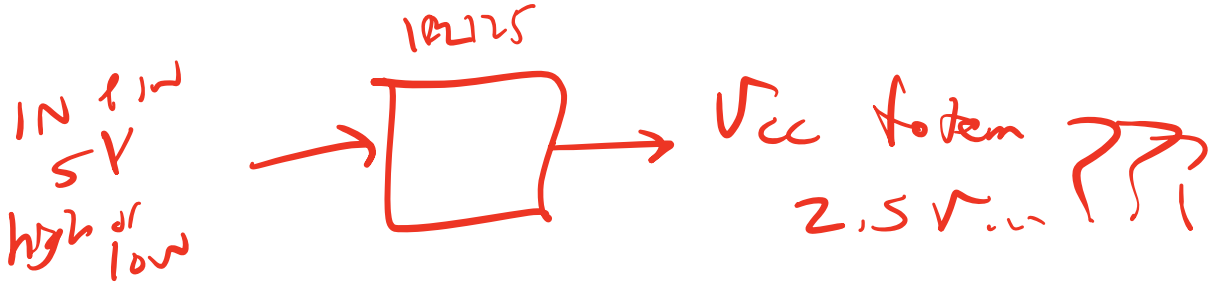
(ISOLATED AT DRIVER CHIP IR2125)

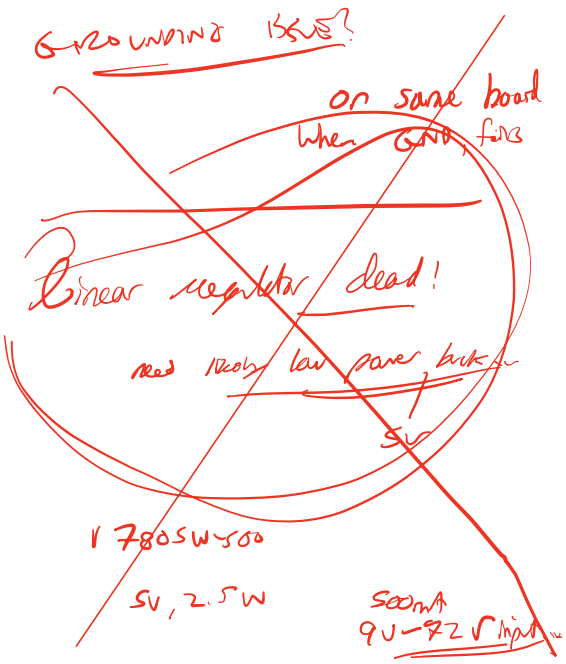
even w/ diode → not works



When 2125 out, good in

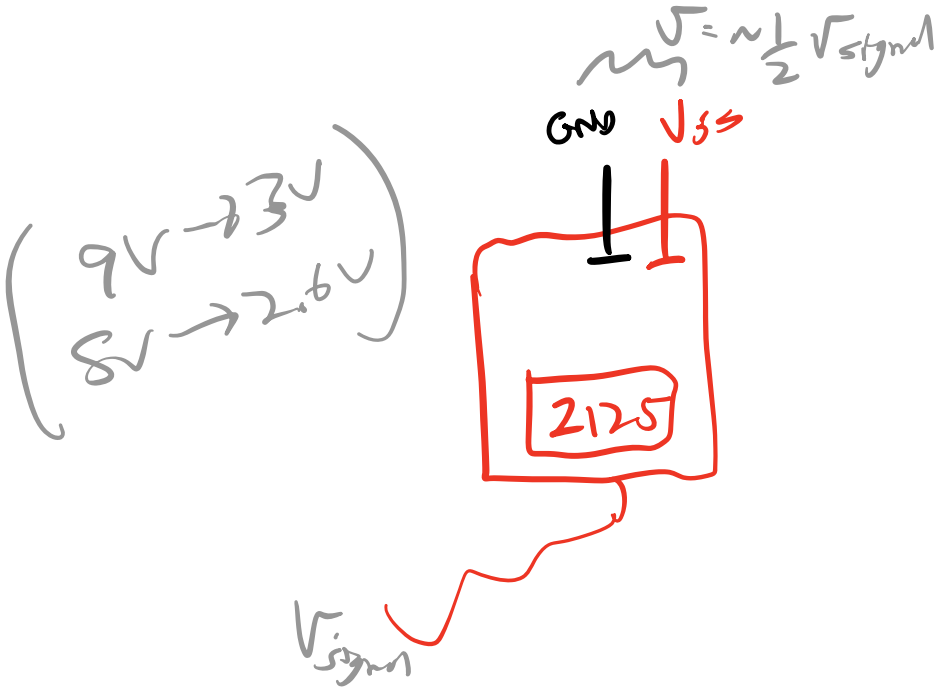






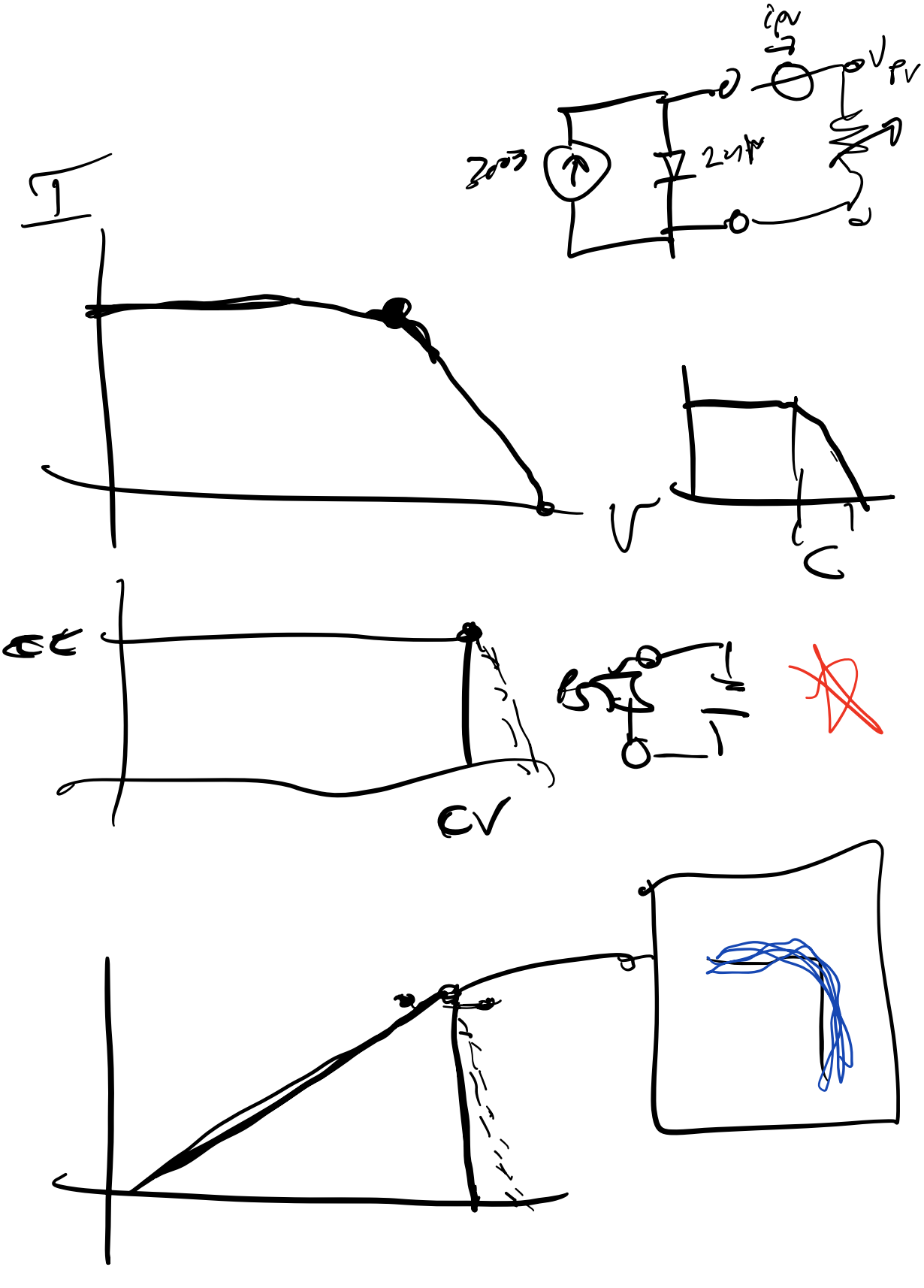
N.; when on separate P.S.

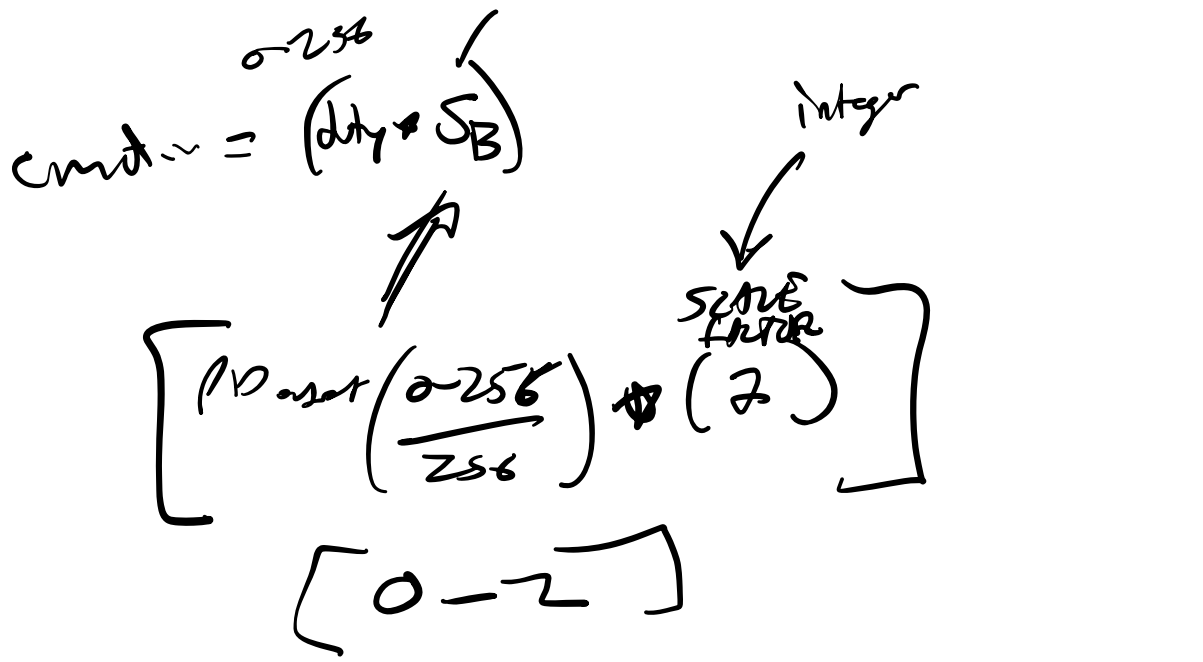
GND, or O.C. on V_{SS} V_{CC}



12/9/23 → 2125 on A, H fried multiple times.. in FET?

Unknown cause, might do CHB


i_{PV}
V_{PV}
200
2 μF
I
V
C
CC
CV



(0-256) (0-2)

cmd max = duty * SB

= 256

256/256 ⇒ 1

256/128 ⇒ *2

((cmd/duty)) * SB side factor = max line

(cmd/duty) ⇒ 0.9

i_{lim}

Wait until i settled ~30 s

4 min/day

1 min/test

C = [ ]	Q = [mL/min]	V	i
	700		
	300		
	1200		
	600		
	1500		

C = 500

5 cell pairs

Unleak spacers

——— cm^2 mem area

——— cm^2 cathode area

electrode type

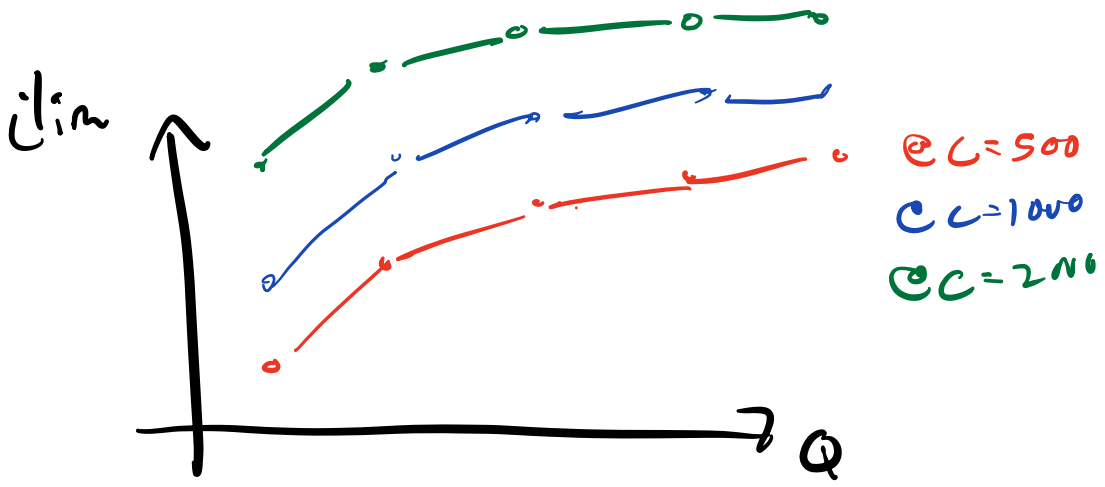
Wait ~

C = [ ]	Q = [mL/min]	V	i
	700		
	300		
	1200		
	600		
	1500		

C = 1000

C = [ ]	Q = [mL/min]	V	i
	700		
	300		
	1200		
	600		
	1500		

C = 2000



$i_{lim} = \alpha \, C \, Q^{\beta}$ fit α, β

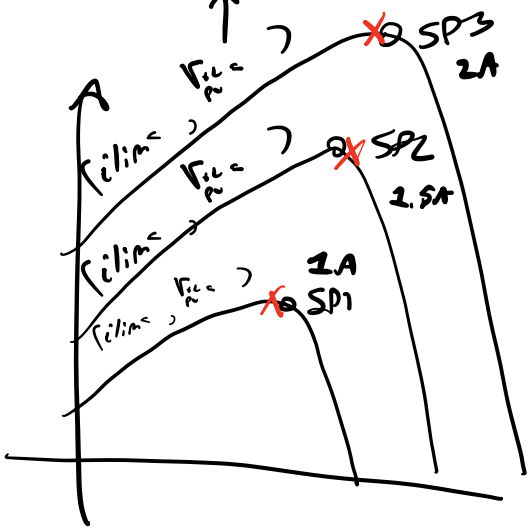
PAPER FOR 6.210 Paper

STEP RESPONSE

2.8A for 3003 power supply

5.21A I_{sc}
20.4V nominal
24V.c

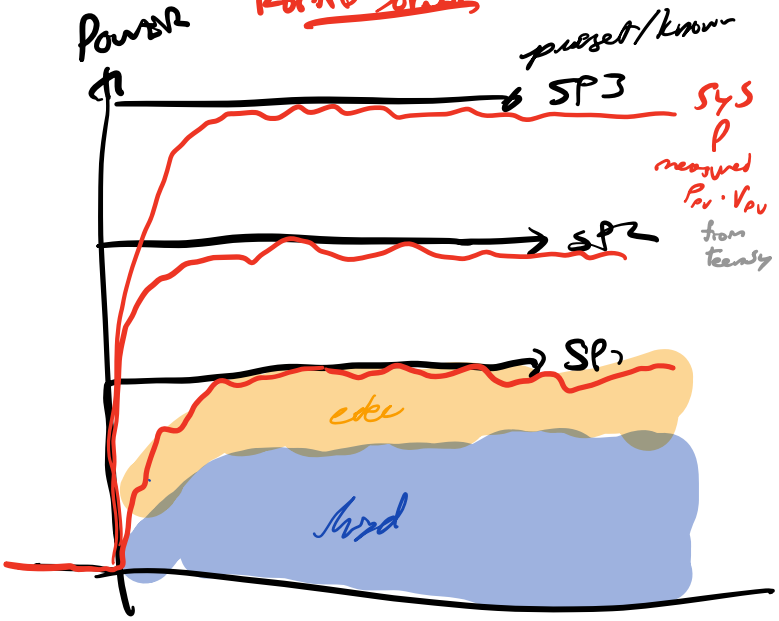
pwrs in w/ multimeter (how)



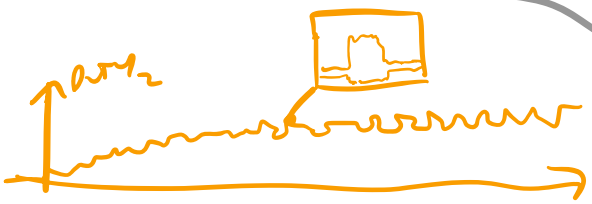
"we are tracking MPP"

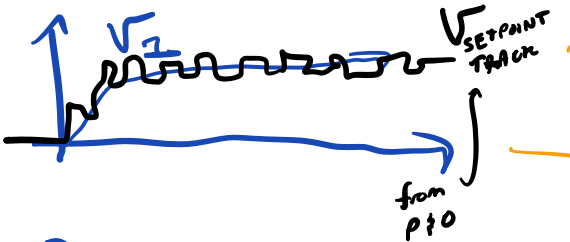
{ (PRESET) 3003 OFF, TRIGGER OFF }

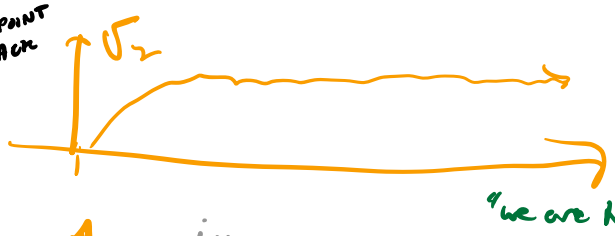
KORAD 3003A

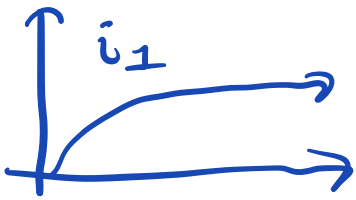


from Peerless

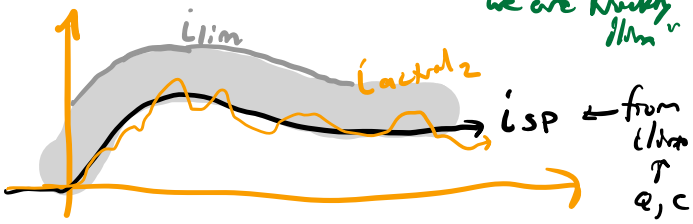


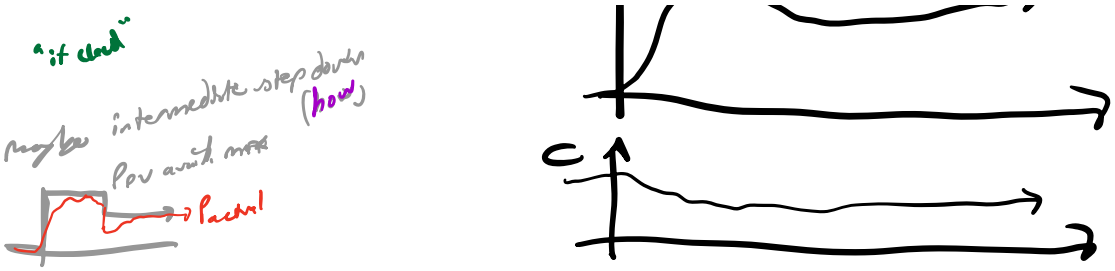


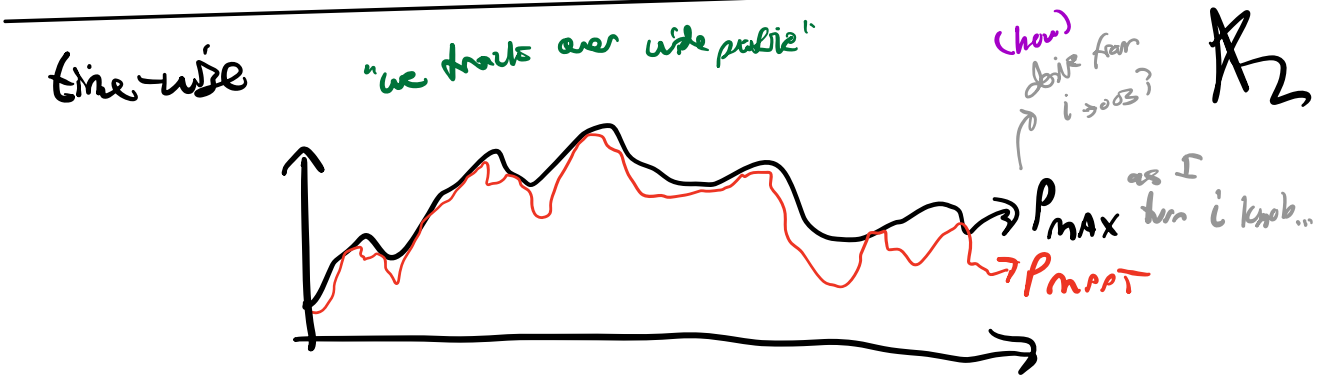




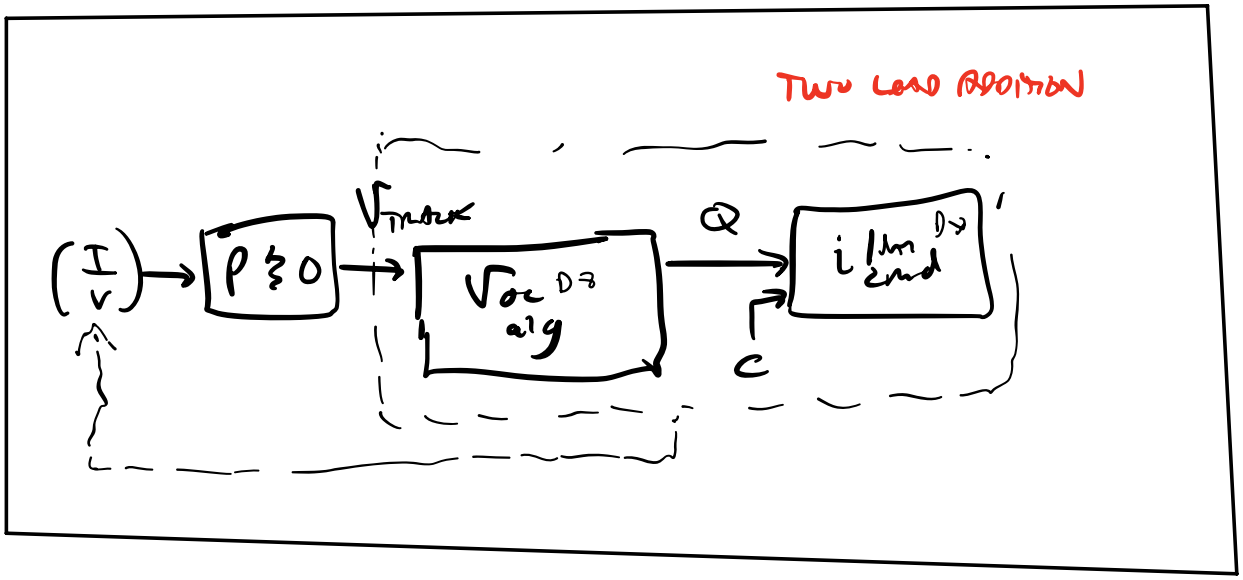
"we are tracking i_{lim}"

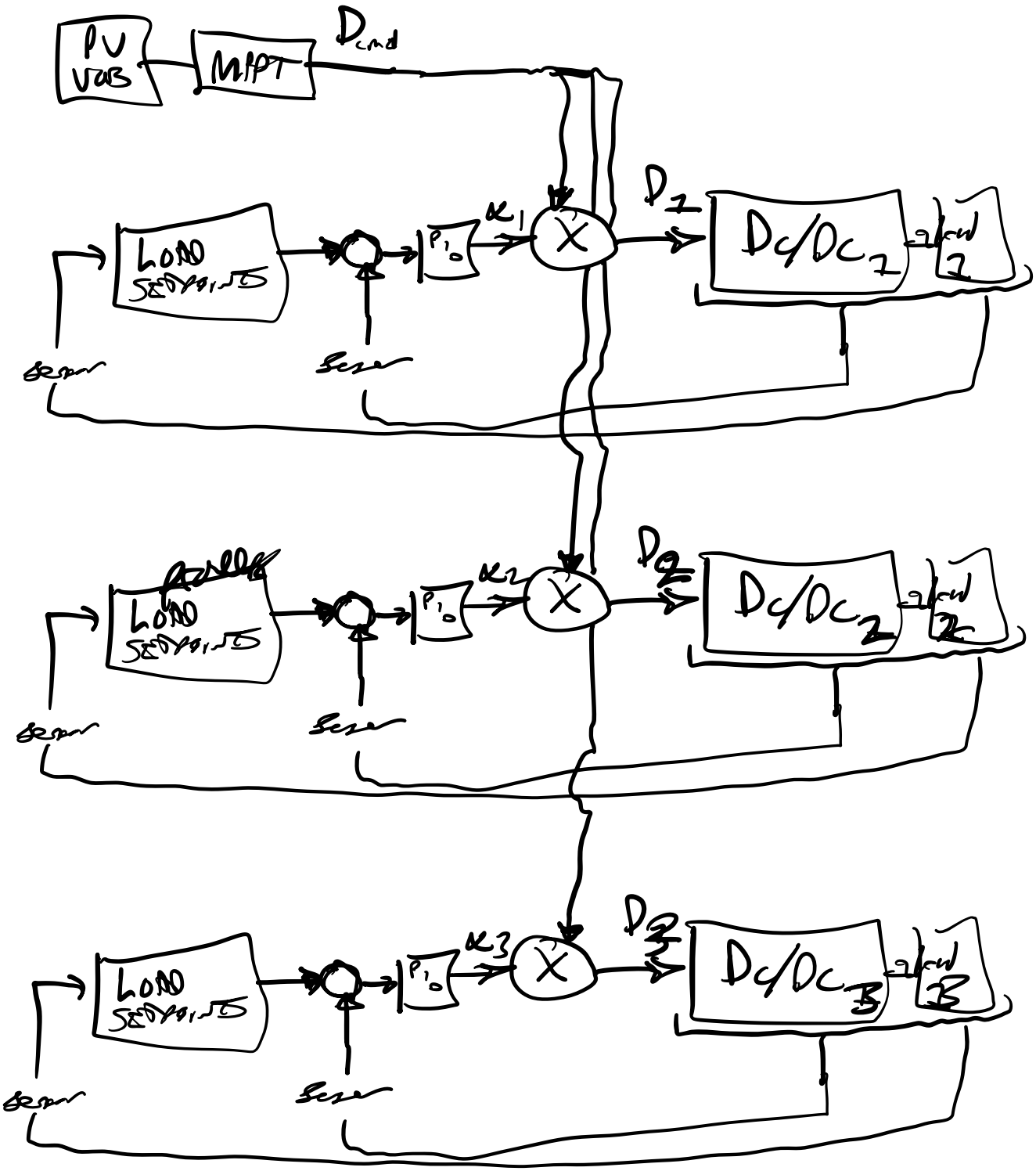


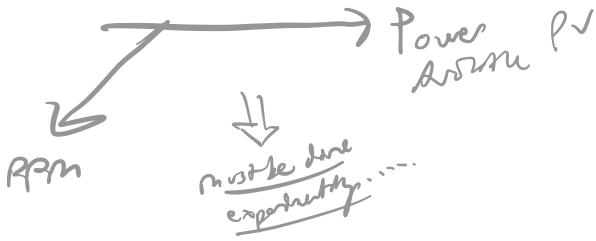




- PID params
- fs




PV
VOB
MPPT
D_{cmd}
LOAD
SETPOINTS
P_{10}
K_1
X
D_1
DC/DC 1
POW
1
LOAD
SETPOINTS
P_{10}
K_2
X
D_2
DC/DC 2
POW
2
LOAD
SETPOINTS
P_{10}
K_3
X
D_3
DC/DC 3
POW
3

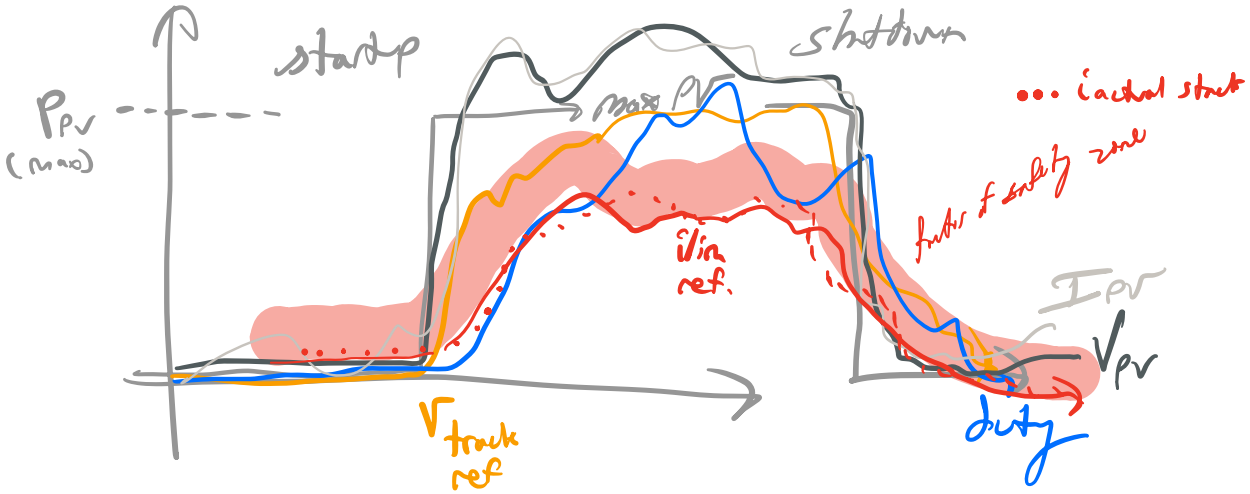


plot % error from this

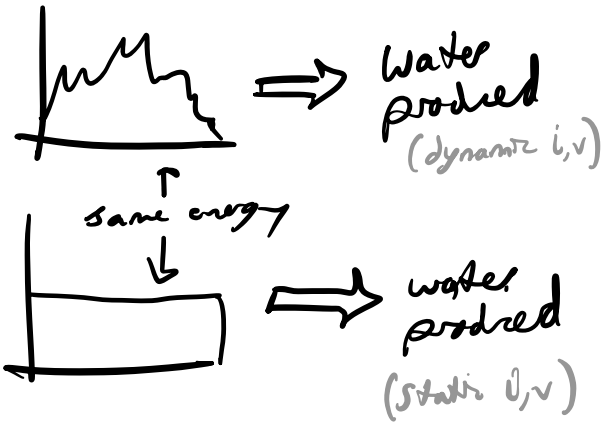
(how to monitor ...)

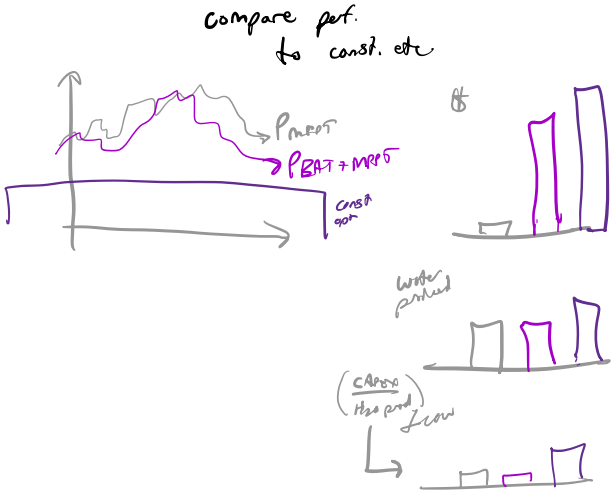
if Fuses turns off...

- STEP RESPONSE (for a given tuning)

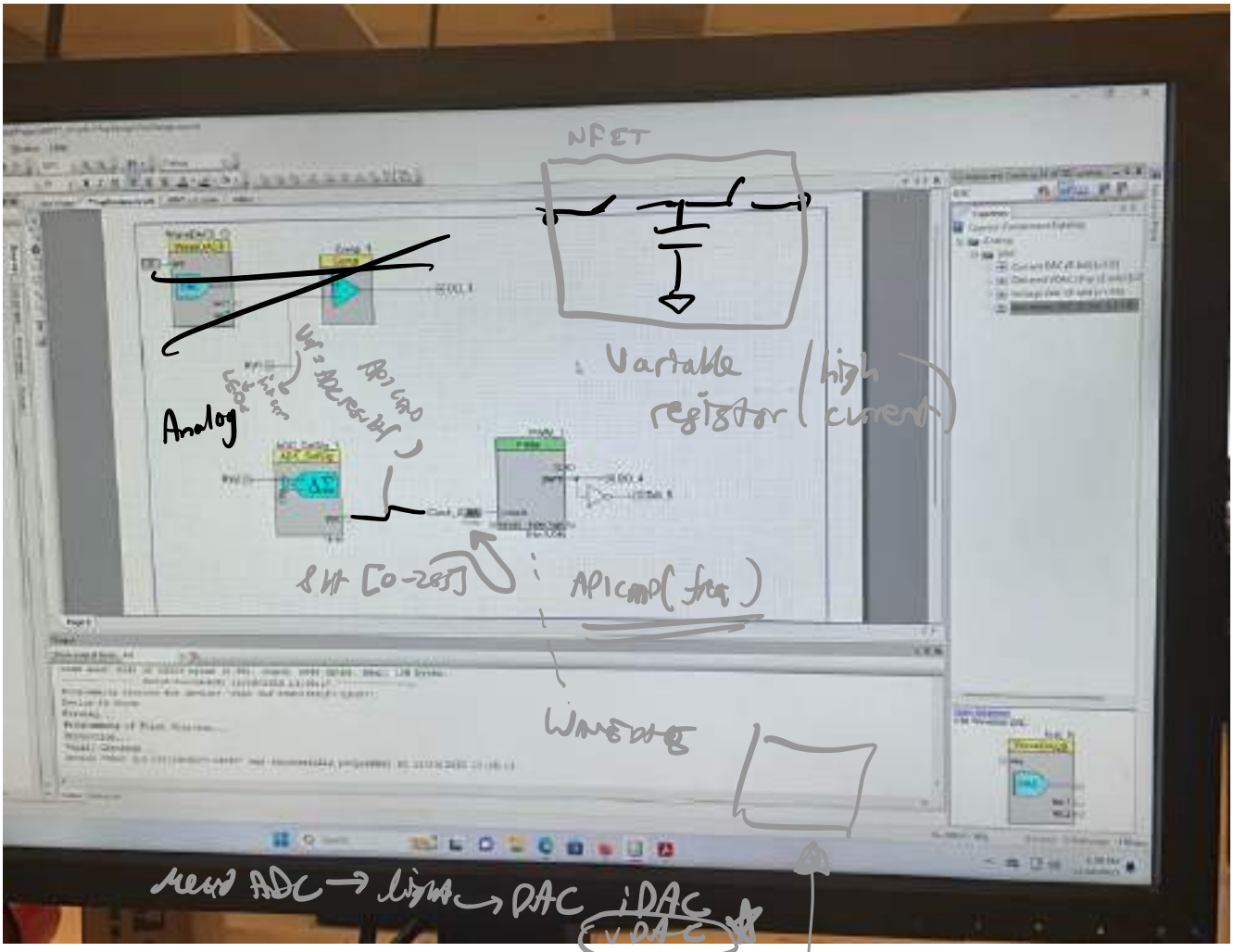


- Methods / metrics to compare ctrl to state of the art?





comparable H2O produced w/o batteries.



VCO

↓

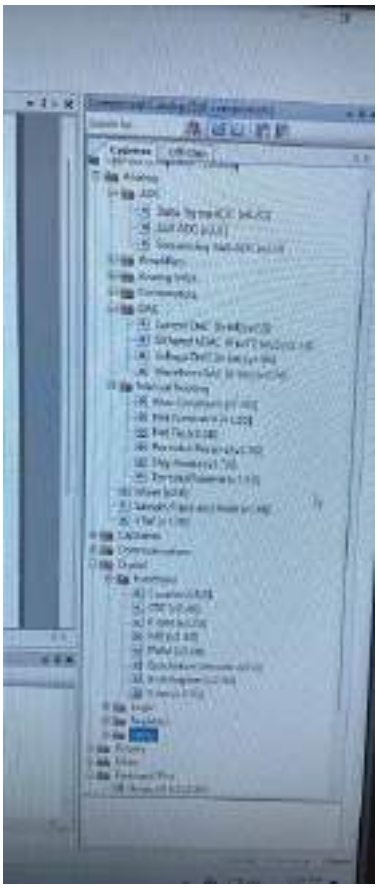
{voltage controlled oscillator}

freq. to voltage converters...

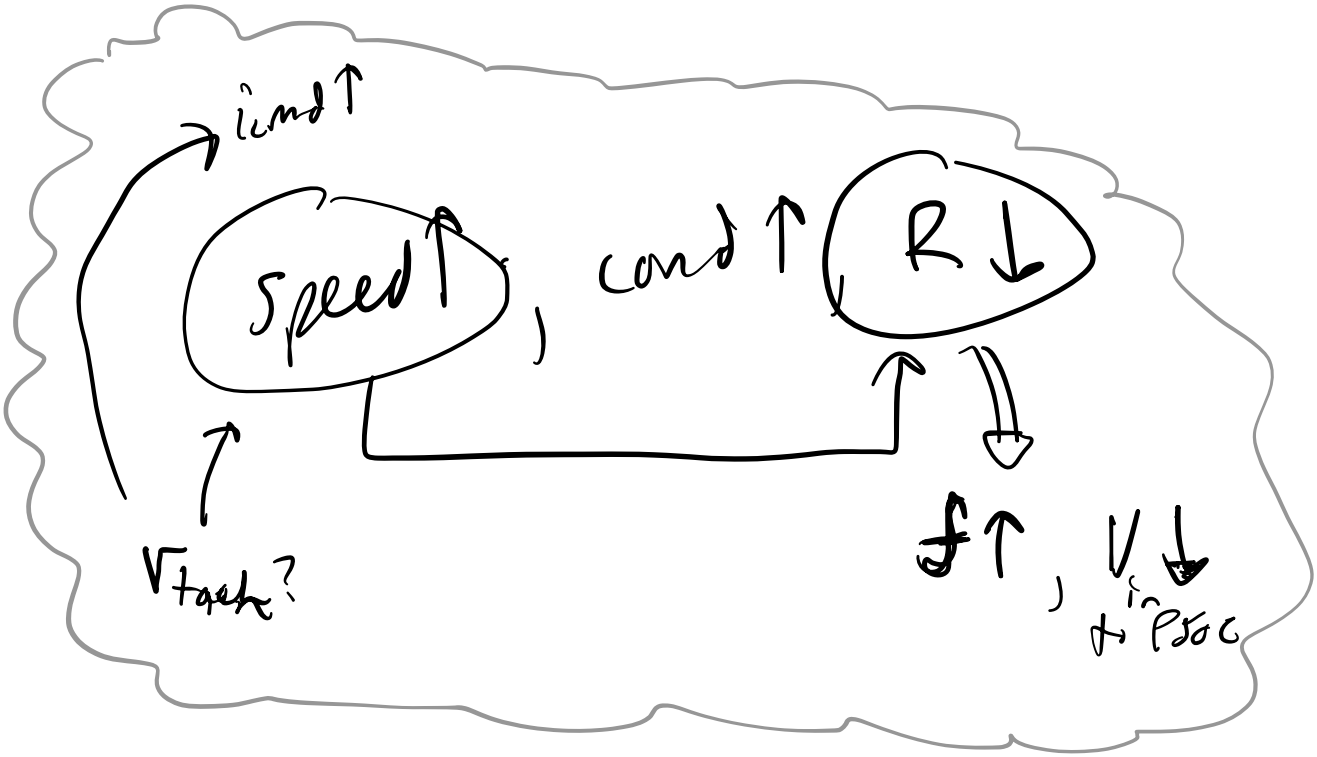
direct memory access

ADC → DMA → Timer → Waveform

PSoC Creator



Clock	8 bit Pwm	Analog V	Digital 32bit	Mapped Value	Meas f
100 kHz	390Hz	2.25V	2,147,483,650	32768	8.2 Hz
					3.05Hz
100kHz		0.98V	841,813,590	12846	7.78Hz
↳ 390Hz					100Hz
		.11V			858Hz
		4.75V			3 Hz
		.23			500Hz

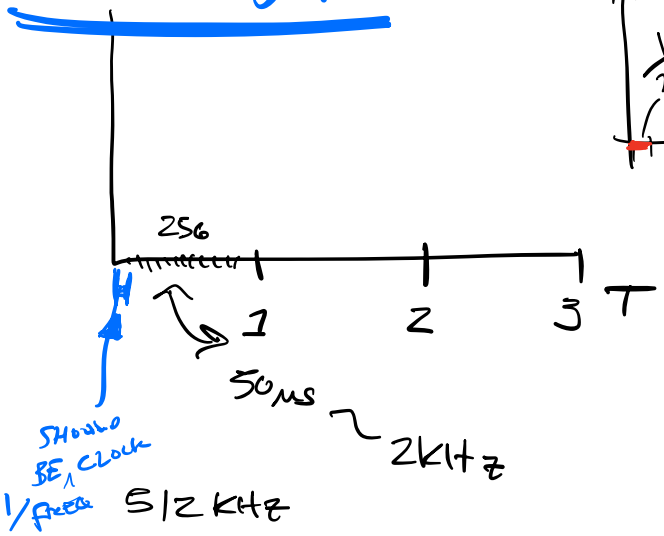


$$f_{desired} \cdot 256 = f_{clock}$$

$$\frac{1}{\left(\frac{\left(\frac{1}{f_{desired}}\right)}{256}\right)} = f_{clock\ required}$$

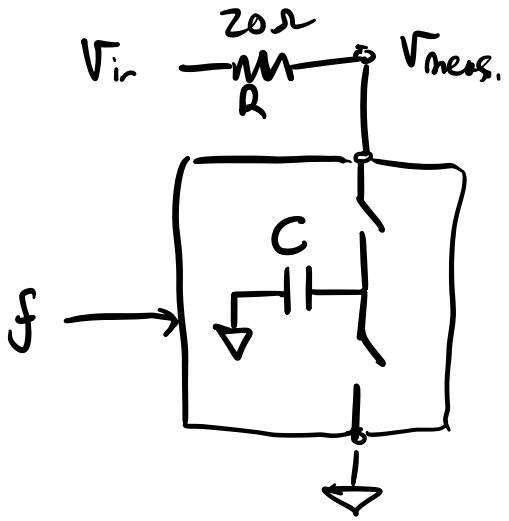
↑ bits

notes on setting PWM



$\left(\frac{1}{2kHz}\right) = T \div 256 = T_{clock}$

$\frac{1}{T_{clock}} = f_{clock}$

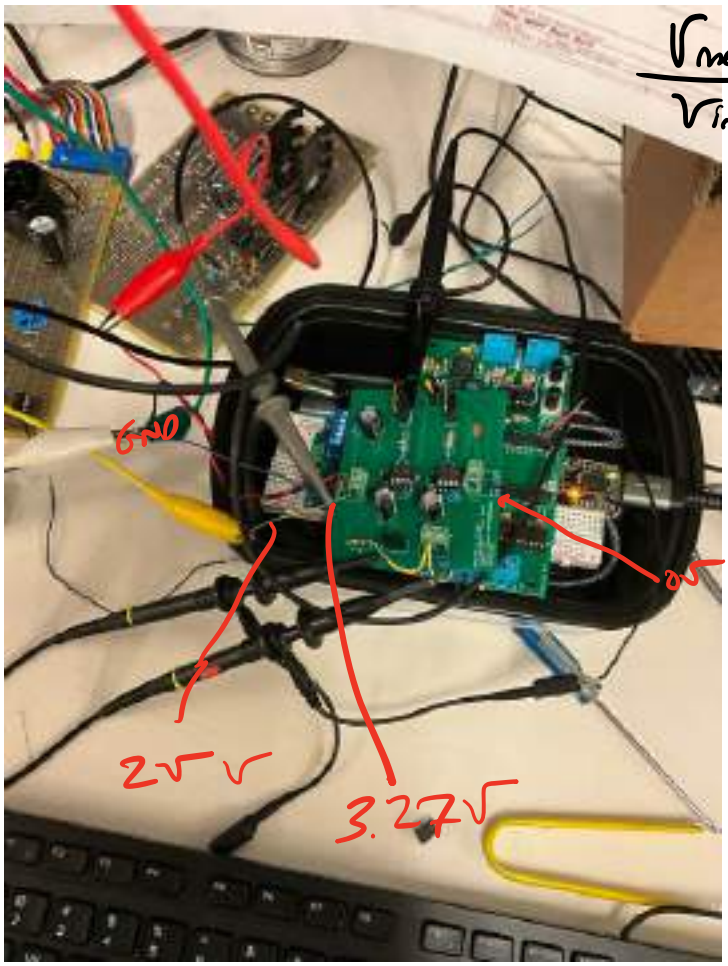


$$V_{meas} = V_{in}\left(\frac{R_2}{R_2 + R_1}\right)$$

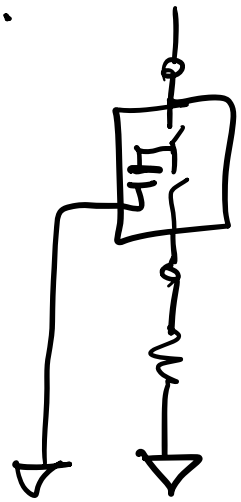
$$V_{meas} R_2 + V_{meas} R_1 = V_{in} R_2$$

$$V_{meas} R_1 = (V_{in} - V_{meas}) R_2$$

$$\frac{V_{meas} R_1}{V_{in} - V_{meas}} = R_2$$

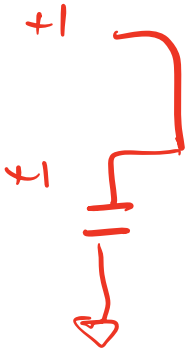


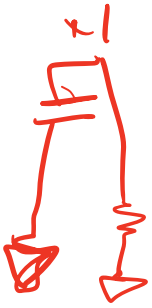
try:



dunno, this is a VT (but is it?)

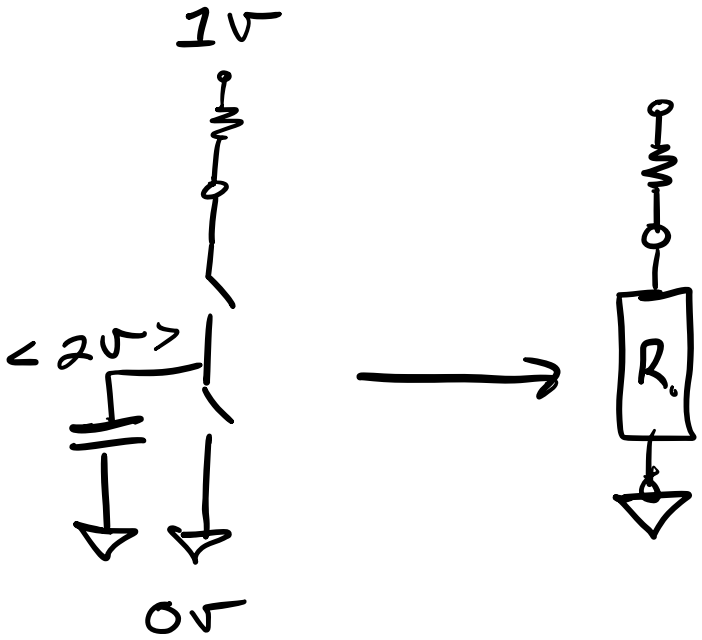
perhaps voltage divider doesn't apply



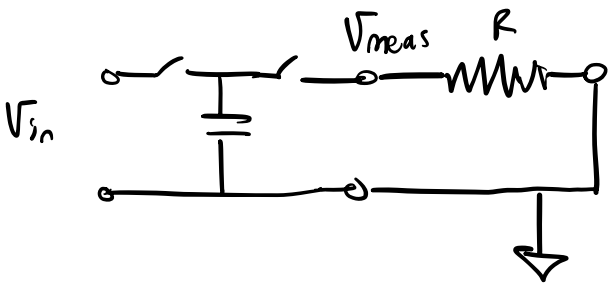


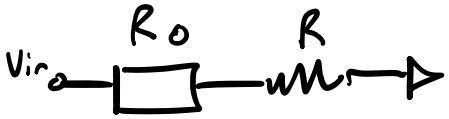
would not change voltage...

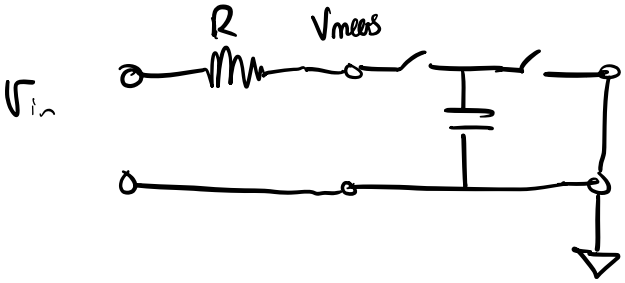
but should consume power?...

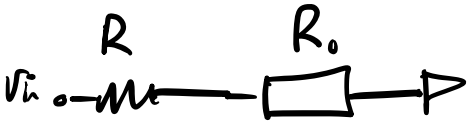


$R_0 \sim \frac{1}{Cf}$









$V_{meas} > V_{in}$ e.g. @ 10 Hz, $C = 0.1\,\mu F$

$D = 0.5$, $R = 10\,k\Omega$

V_{in} =	V_{meas} =
1	2.14
2	3.08
3	3.89
4	4.68
5	5.41

When I expect

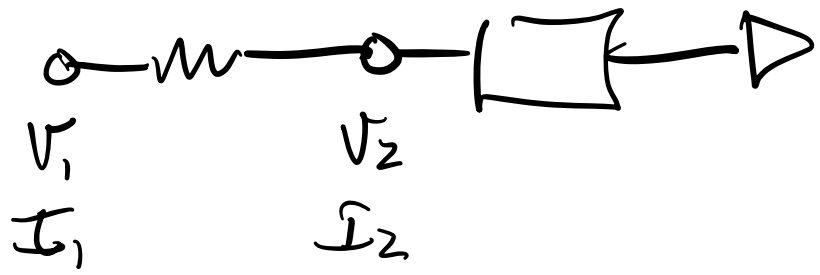
$$R_0 = \frac{1}{Cf} = \frac{1}{(0.1e{-}6)(10)} = 1\,M\Omega$$

so,

$$V_{meas\ expected} = V_{in}\,\frac{R_0}{R+R_0} = (1)\left(\frac{1\,M\Omega}{10k\Omega + 1M\Omega}\right) \sim .99\,V_{in}$$

"buffer" / variable resistor...

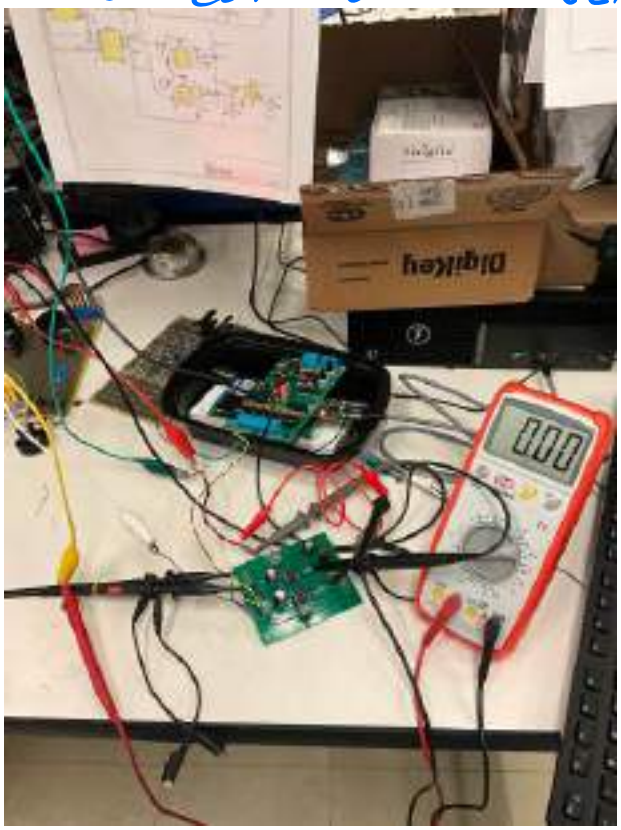
$P_{in} = P_{out}$



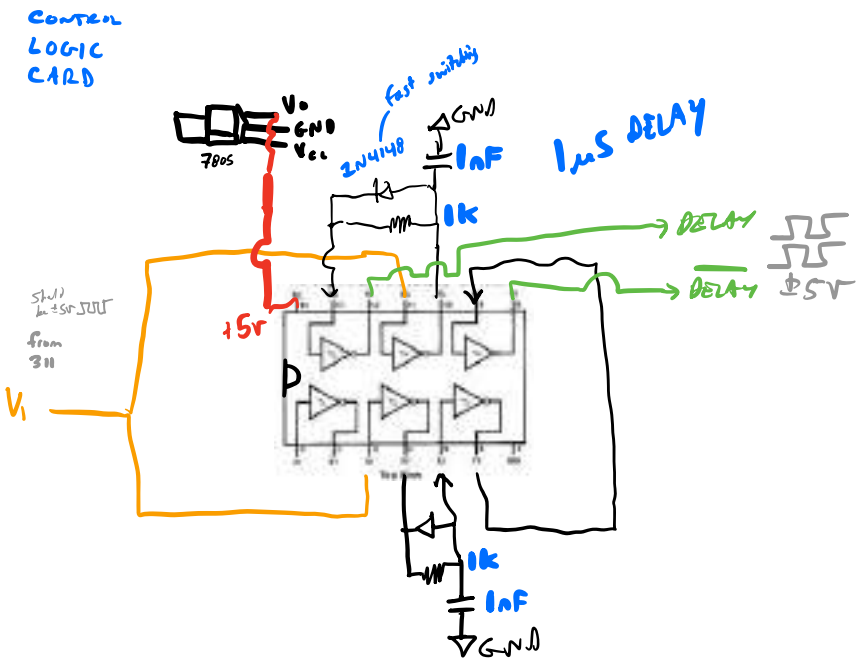
$I_1 = I_2$ ... perhaps it changes w/ freq?

same current w/ and w/o sw cap.

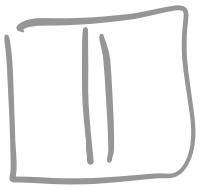
SW cap VAR R (EXP)



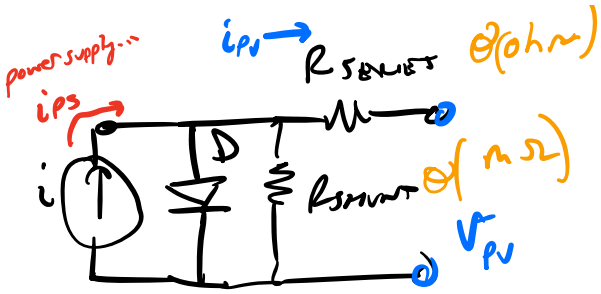
worry about this later...



I can add breadboard + PCB... →



PV model



$i_{sc} R_s << V_{oc}$

$i_{sc} \sim \frac{30mA}{cm^2}$

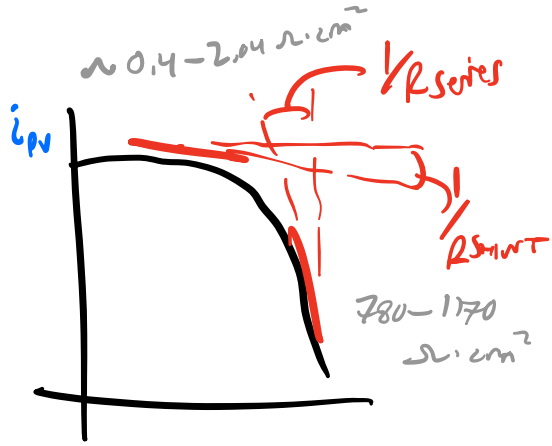
Typically $R_{SHUNT} \sim 100\Omega \cdot cm^2$

$V_{oc} \doteq 0.6V$

$R_s << 2\Omega \cdot cm^2$

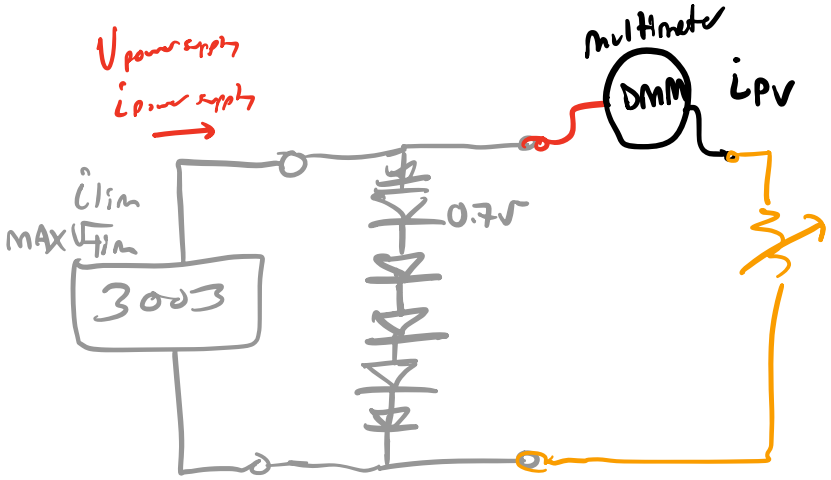
100 W Panel ; 18V
6A @ 12VDC

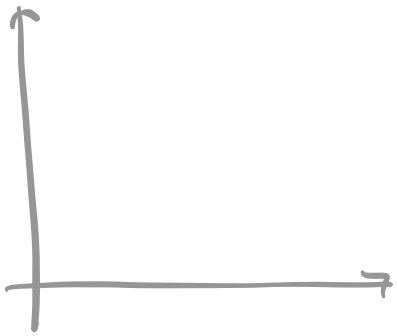
6839 cm^2



[2016 Niasse et al.
Optimization of Electrical Parameters CdS/CdTe Thin Film ...]

e.g., w/ a potentiometer and multimeter





@ $R_{FULL\ S.C.}$, $i=0$, $V=max \rightarrow i=0$, $V \doteq 1.5V$ from diodes?

x6 D no. regulated diodes

$i = 0.1$	V
D = 6	5
D = 20	14.2

POWER SUPPLY

D = 20

$i_{lim} = 0.3A$

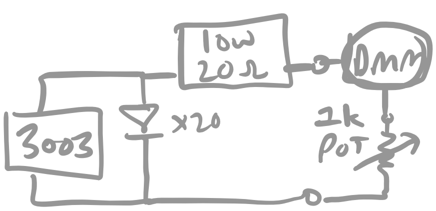
PV V	PV i
13.6	0
13.4	0.03
13	0.05
9.9	0.11
0.3	0.12

now w/ 20Ω 10W power R series

$i_{lim} = 0.10$

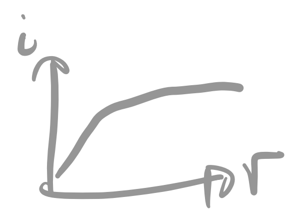
1k POT

PV V	PV I
14.2	0.01
13.9	0.02
13.8	0.03
13.5	0.04
13.2	0.05
12.9	0.06
12.6	0.07
12.5	0.08
12.2	0.09
11.8	0.10
9.9	0.11
4.9	0.12
2.7	0.12+ ...



"[illegible]" apparently

lamp ~260mA "~24V" MAX



BULB

0.05 A → 2.52 V out ? ...

inverse signal perhaps ? ...

from 0.05A
2.52 raw
1.72 after divider

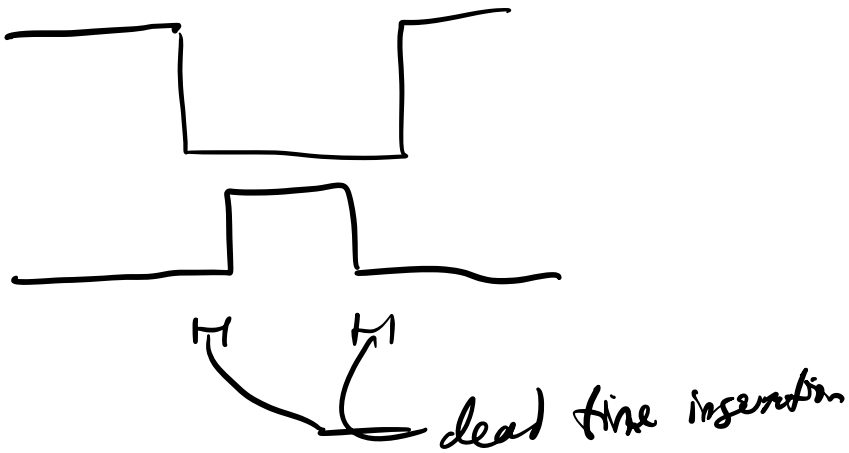
0-5V
0-11A ? ...
11-0A ? ...

.450 450mV/A ...

→ 0.225 V expected ...

4.705 ⟹ 3.15^15

~~SAM~~
2.52, 1.72

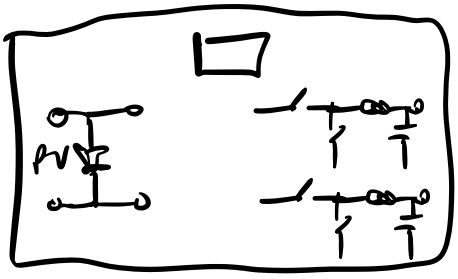


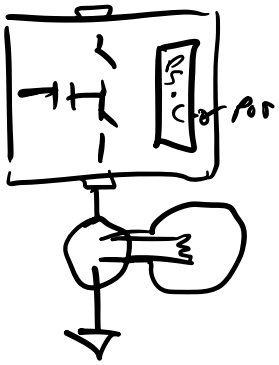
MVP (12/3/23)

MPPT-BUCK CONVERTER

high current SW. cap variable load

- data monitoring / visualization
- Ports & observ MPPT





- ideally 2 buck MPPT

TO DO:

- calculate expected efficiencies
  - buck
    - FETs (f/sw)
    - ohmic losses
      - driver losses?
  - V drops $P = i^2R$ $i^2 V/R$
  - CPU draw
  - SW cap
  - light

TODO: pot → f → expected R out... (add delay on...)

- measure experimentally (V_{in} I_{in}) (V_{out} I_{out}) η

make breaks ?

- calc/measure disruption speed?
- show startup/shutdown?

- TLO disclosure → MPPT PVDD (ctrl. wgs.)
  → CONT. VIRT LOAD SENSOR

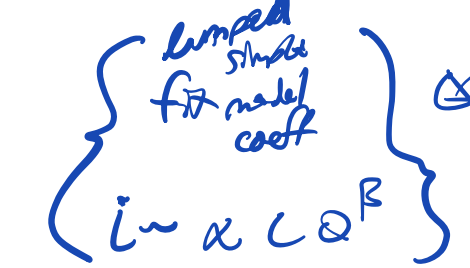
- MPPT algorithm formulate!
  on Teensy
- validate { V regulators, i sensors, V sensors } { PWM signal teensy }

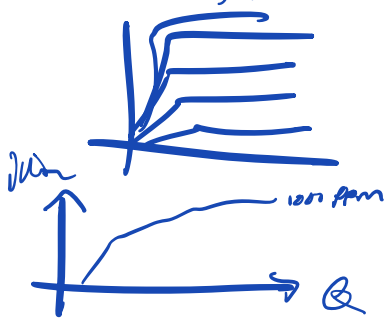
Sense ← [ADC] ← three PWM

supervisory off ctrl.

for added delay (+t)
(maybe keysight scope)

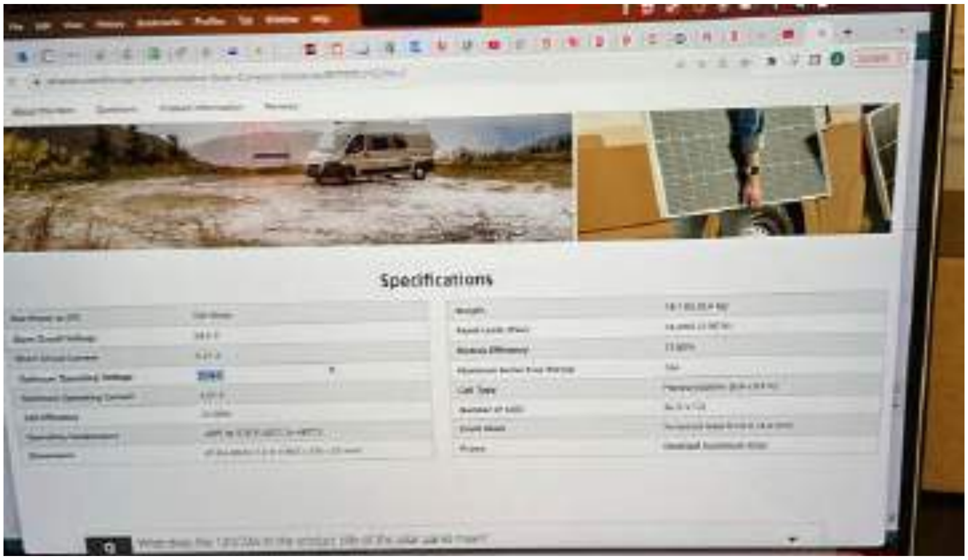
- to do: 12/9:
  - sensor recording to x/x. or something
  - Δi_1 sense
    Δi_2 sense
  - ΔC sense
  - Δ Q sense
  - fix channel A 2125 driver failure
  - assemble stacks, conduct iV sweeps on one card, multiple flows





  - i control alg. PID
    w/ setpoint from $i_{in} \leftarrow Q, C$

Kind



≈12-16V
O(100 mA)

0.54 mm spacer
0.65 mm

- to do 12/12/23

10A ✓ o ilim stacks coeff.

✓ o i calibration

5cP
0.6 void frac
0.45 avg porosity

→ steve on; ask ✓ o to bring in system

12P

• figs

✓ o 2125 dyly; current rating on PCB?
(1.2A max per channel)
but then 2.4 on Vdd

charge/
discharge?

8:20! → tune i sensor / recalibrate so reorient is most accurate

→ see ilim response?

→ try for a step.

if not done by ILP →

call it / use current results

→ tune i cmd PID (kp, ki)

1P

G2228 Totem

- LAB → Card #2 (backup)
  → PSoC variable Resistances ...

- ½Voc record (?) step for different Voc targets (show clamp settings)

- MPPT tracking.

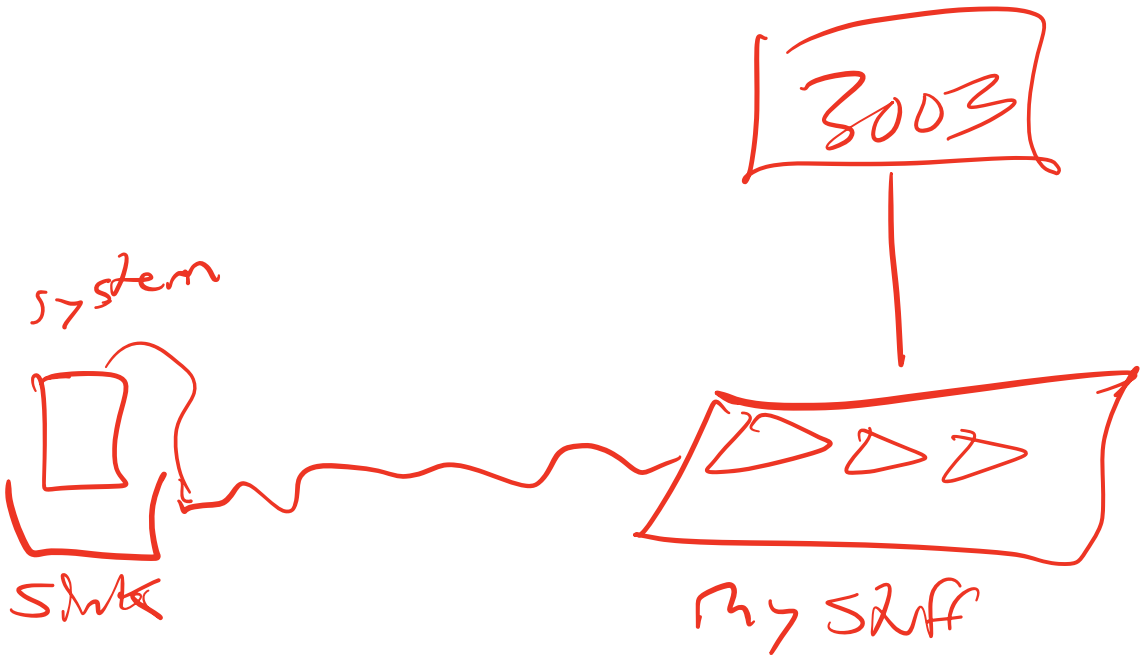
⟹ writeup: → intro
  → diagrams — BLOCK CTRL etc.
  RQ
  → methods:
    → calculations DRs
    → component choices
    → schematic
    → exp. setup

→ results

- Variable R
- "PV Panel"
- step responses

→ discuss/design.

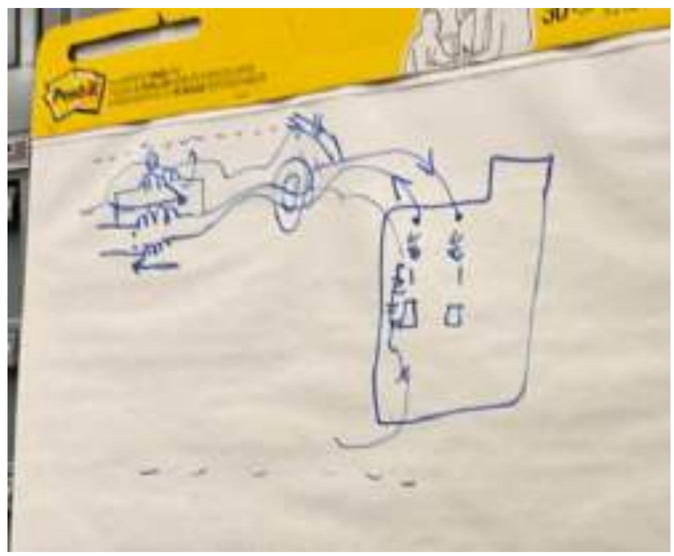
- 22 AWG → 5A
- PCB trace 1.27 mm → 0.050" ✓ ✓
  for 3A



- 2/25 — Common Mode Choke

- 2/28 app note Lattson

Bonshire



enable 0 : ya sy

ctrl write(value=1)

$2^0 \rightarrow 1$

$2^1 \rightarrow 2$

$2^2 \rightarrow 4$

$2^3 \rightarrow 8$

if ——

ctrl rgwte( )

---

if